Development of a Trigger System for High Energy Particle Beam Tests of Diamond Detectors

Undergraduate Honors Thesis

Presented in Partial Fulfillment of the Requirements for Graduation with distinction in the Department of Electrical and Computer Engineering at The Ohio State University

By

Joseph Warner

The Ohio State University

November 2015

Dissertation Committee:

Steven Bibyk, Advisor

Harris Kagan, Co-advisor

Abstract

In high energy physics, it is often important that devices used to perform experiments are radiation tolerant. Diamonds stand out as a particularly radiation tolerant material capable of withstanding radiation levels of $1.8x10^{16}$ particles per cm^2. Recently it has become important to study the properties of CVD diamonds in high radiation environments with event rates beyond 1 MHz/cm^2. A new trigger system was developed for performing high rate beam tests of diamond detectors. The new system was designed to combine all of the components of the coincidence logic and trigger logic into a device. The trigger system collects and transmits data in real-time to allow operators to make adjustments to experiments while they are collecting data. The prototype trigger system successfully controlled and collected data in a beam test at the Paul Scherrer Institute in Villigen, Switzerland.

Dedication

This document is dedicated to my family and supportive friends.

Acknowledgments

I would first like to thank Prof. Harris Kagan, one of my co-advisors, for allowing me to perform this research. I would also like to thank Dr. Shane Smith for mentoring me throughout my two years in the research group. Additionally, I would like to thank Prof. Steven Bibyk, one of my co-advisors, for mentoring and supporting me in many endeavors in and outside of the lab.

For his assistance and guidance in the development of the firmware and software for the trigger system, I would like to thank Jason Moore. And for his writing of the firmware for the test system, I would like to thank Jack Bargemann.

Thanks to the vision of Felix Bachmair from ETH Zurich, this project became a reality through his development of the specifications of this new trigger system.

I am appreciative of the financial support that I have received from the Ohio State College of Engineering and the Ohio State University Undergraduate Research Office.

Finally, I would like to thank the other members of the Ohio State University High Energy Physics program who have educated me and assisted throughout my time working with Prof. Harris Kagan.

Table of Contents

List of Figures

1. Introduction

In high energy physics, it is important that all devices used to perform experiments are radiation tolerant. Diamonds stand out as a particularly radiation tolerant material capable of withstanding radiation levels of $1.8x10^{16}$ particles per cm^2, which exceeds the current projected maximum radiation fluence levels in the Large Hadron Collider [1] [2] by an order of magnitude [3]. Diamond is also particularly useful as a detector of charged particles by ionization [3]. So far, research has been performed on chemical vapor deposition (CVD) diamonds as detectors [4].

To characterize these diamond detectors, they are often subjected to what are called beam tests in high energy particle beams. Currently a 120 GeV beam of protons at CERN and a 250 MeV/c pion beam at the Paul Scherrer Institute (PSI) [5] [6]are used for these beam tests. These beams are used because the energy levels at these facilities are closer to those in a high energy physics experiment than conditions possible in the laboratory. Additionally, higher energy beams also permit access to important experimental parameters [7].

When measuring properties such as efficiency and spatial resolution, a device under test requires a precise reference measurement of the location of the incident particle tracks. The best tool available for this is a beam telescope that measures the path of each incident particle including their intercept and angle achieving position resolutions on the μm and mrad scale [7]. Commonly used detectors in beam telescopes are silicon microstrip detectors, which provide space points for tracking [7]. These silicon telescopes are used to

find how the particle was moving while passing through the layers of silicon and the CVD diamond.

Recently it has become important to study the properties of CVD diamonds in high radiation environments with event rates beyond 1 MHz/cm^2. For future diamond detector systems to be successful in measuring beam positions or to take high time resolution samples of the beam flux, they must be proven to operate well at high rates. To improve the reliability and reproducibility of the test setup under such high rate tests, a new trigger system had to be developed.

A trigger system is a system which quickly decides which events in a particle detector to record when only a limited subset of the total events can be recorded. These systems are necessary primarily because of limited computing power and limited data storage. Trigger systems often have a trigger rate many orders of magnitude less than the event rate. Modern accelerators have event rates greater than 1 MHz and trigger rates are often below 10 Hz. To be able to determine which events to record, trigger systems require fast FPGAs to quickly determine when events occur, when to record an event, and when to notify all other devices in the system to collect data.

2. Existing Systems and the Need for a New Trigger System

The EUDET [8] JRA1 Trigger Logic Unit (TLU) [9] was developed to provide a high-speed TLU to collect data to support the research and development of new detectors in Europe for the International Linear Collider [10]. Since it was created, it has been used in beam tests at accelerators throughout Europe. The TLU has LVDS [11] or TTL [12] interfaces to the beam-telescope readout and all devices under test, negative fast NIM [13] level signal interfaces to the beam-trigger and a USB interface to the DAQ [9]. It was designed to use an off-the-shelf FPGA board to speed development and went through one major revision after being created. The device was designed as part of the JRA1 collaboration and fabricated by the University of Bristol HEP [14].

While the EUDET JRA1 TLU met the requirements of the original project, several key problems with it were identified over time. The largest issues in the system were

1. A lack of the ability to prescale triggers in the TLU. This led to the TLU having to rely solely on other devices in the system to know when an event should be recorded. With prescaling, operators can choose how many events they want to ignore before choosing to record an event all within the TLU.
2. No separate pulser input existed requiring operators to tie pulser operation to another input.
3. There were many long cables to the display unit before the readout would reach electronics. This introduced unnecessary delays in the system leading to a different view at the display unit compared to what was currently happening in the system.

4. Using the JRA1 TLU required the use of rack of additional equipment to handle the trigger.

The problems with the existing TLU lead to a need for a new TLU that would fix these issues, implement updated trigger logic, and provide the ability for the researchers to make a variety of upgrades to the system over time.

3. Design of the New Trigger System

A new collaboration group was started in the summer of 2014 between ETH Zurich [15] and The Ohio State University to develop an improved TLU and supporting software. This system aimed to solve the listed problems with the EUDET JRA1 TLU as well as to provide updated trigger logic. A system overview (Figure 1) for the originally designed system included a data acquisition computer collecting data from the PSI46 [16] and DRS4 [17] modules provided by ETH Zurich. Additionally, the system called for a separate laptop to control the configuration of the system and provided limited readout capabilities during the run.

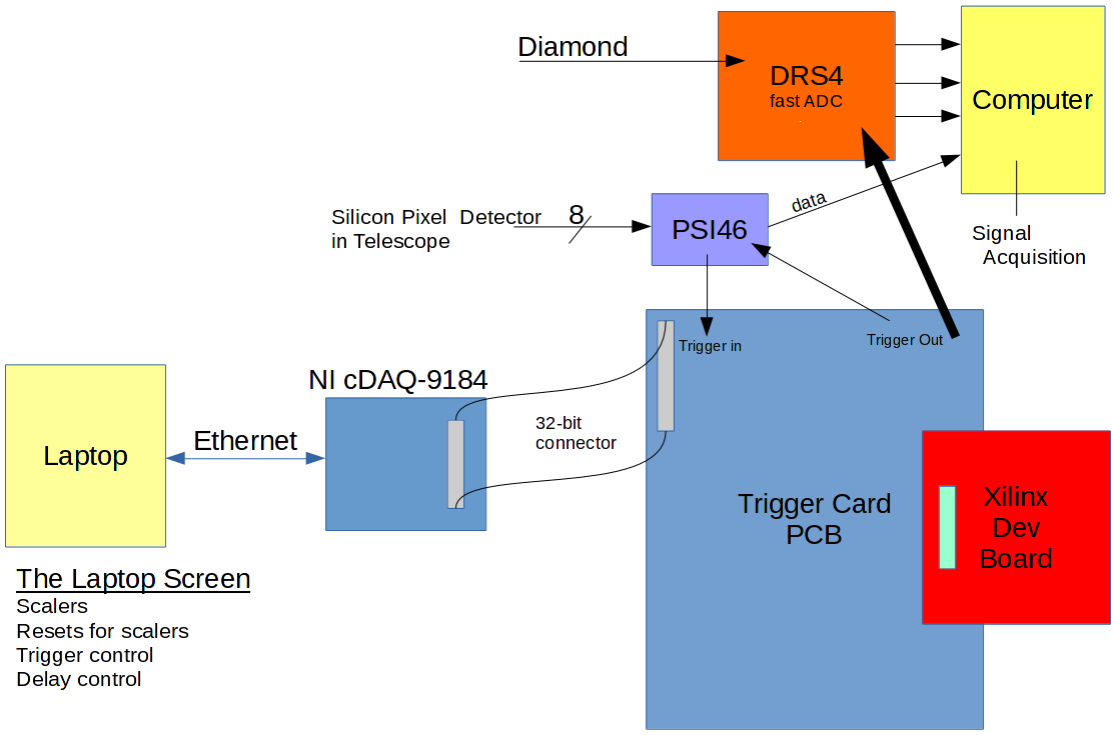


Figure 1: Original system diagram

3.1 Trigger Logic

The updated trigger logic (shown in Figure 2 and Figure 3) includes many more output triggers than the EUDET JRA1 TLU. Figure 3 includes the specific dataflow path through the coincidence unit. It also includes a built-in beam current monitor so that an additional hardware component could be eliminated.

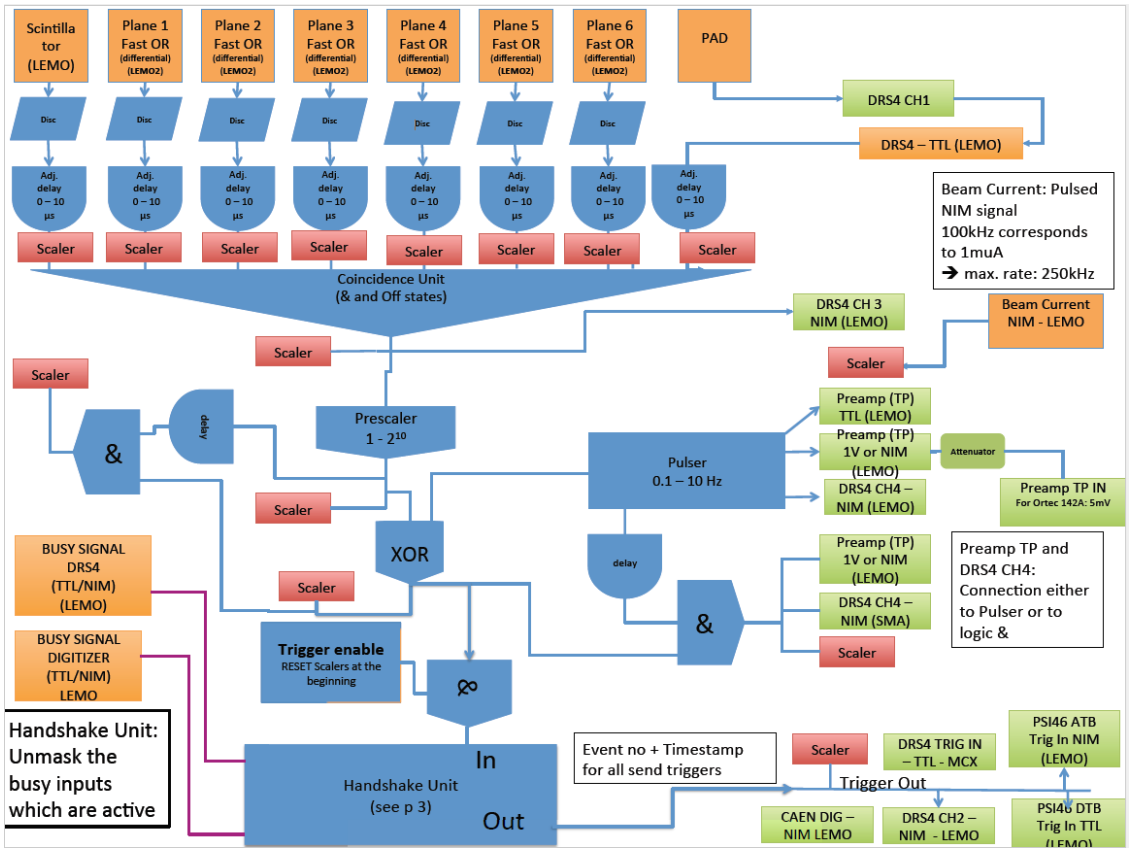


Figure 2: Trigger logic for the new TLU with the coincidence unit

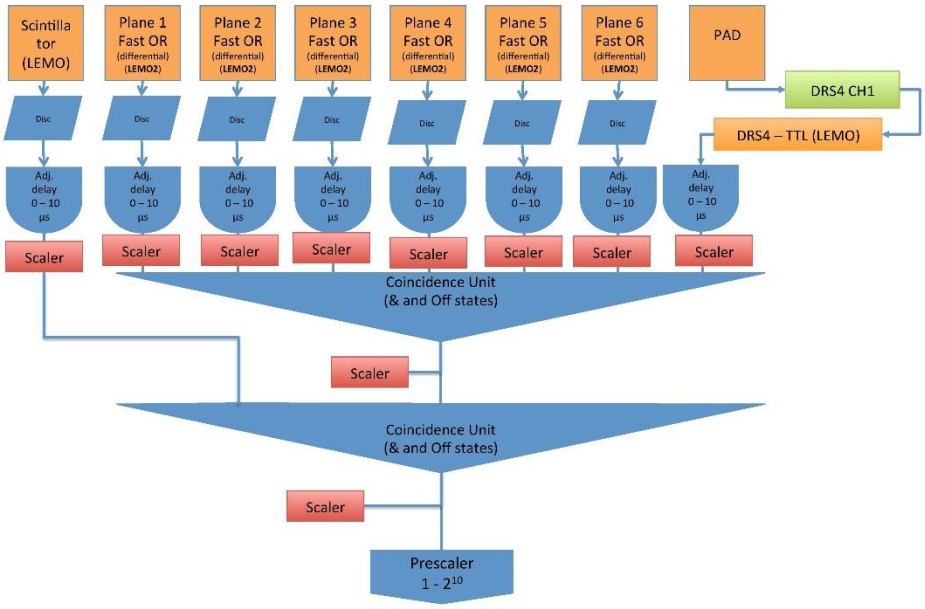


Figure 3: Detailed view of the coincidence unit's logic

The new system is designed to handle event rates far in excess of 1 MHz with trigger inputs on the FAST OR planes, PAD, and Scintillator varying in width from about 10 ns to 25 ns. Each trigger input is specified to be able to be independently delayed and counted before passing into the Coincidence Unit which is a user-maskable AND function. While the above diagram shows only 6 FAST OR planes, a decision was made to build in 8 FAST OR planes to allow for future changes in the experimental setup. The coincidence unit outputs a trigger to the experiment and outputs to the prescaler which determines how many events to ignore before an event may be recorded. Inside of the coincidence unit are two stages: stage one is a user-maskable and gate for all planes of the telescope and stage two where the coincidence of stage one is ANDed with the scintillator's output. These stages allow the operators to see if the telescope is aligned with the scintillator by

comparing the rates of coincidence through the first and second stage. The prescaler then outputs to the trigger logic which determines when an event meets the criteria necessary to be collected. That criteria is that only one event may be collected whenever the pulser triggers at a user-configurable rate of 0.1 Hz to 10 Hz.

The other inputs to the system from the experiment are the beam current which is a frequency counter that converts an input frequency from the beam line into a measurement of the current, and the busy signals which are inputs to the handshake unit. The handshake unit is logic, shown in Figure 4, which determines when data can be collected by data acquisition systems and to only send trigger outputs when all inputs are driven low. The busy signals are user-maskable similar to the coincidence unit and can be configured during runtime.

3.2 FPGA Selection

For selecting an FPGA for the system there were two primary criteria: high speed fabric (>100 MHz for all internal devices) and a high pin count. Additionally, we required that an off-the-shelf evaluation board would be needed due to the complexity and cost of implementing a FPGA on a board. At first, a Xilinx [18] Spartan VI [19] board was chosen due to its small size and low cost. However, after further evaluation of the board it was determined that the board had insufficient pins to handle all of the required input and output pins. Additionally, the block RAM in the fabric of the device was determined to be too slow to use for the purposes of the trigger logic.

After further research into available off-the-shelf boards, the Xilinx AC701 Evaluation Board [20] for the Xilinx Artix-7 [21] family was chosen due to its high pin

count FPGA mezzanine connector (FMC) and the FPGA's higher fabric speed (up to 400 MHz for block RAM). The FMC connector would allow us to rapidly develop a mezzanine board for interfacing the input and output ports to the FPGA.

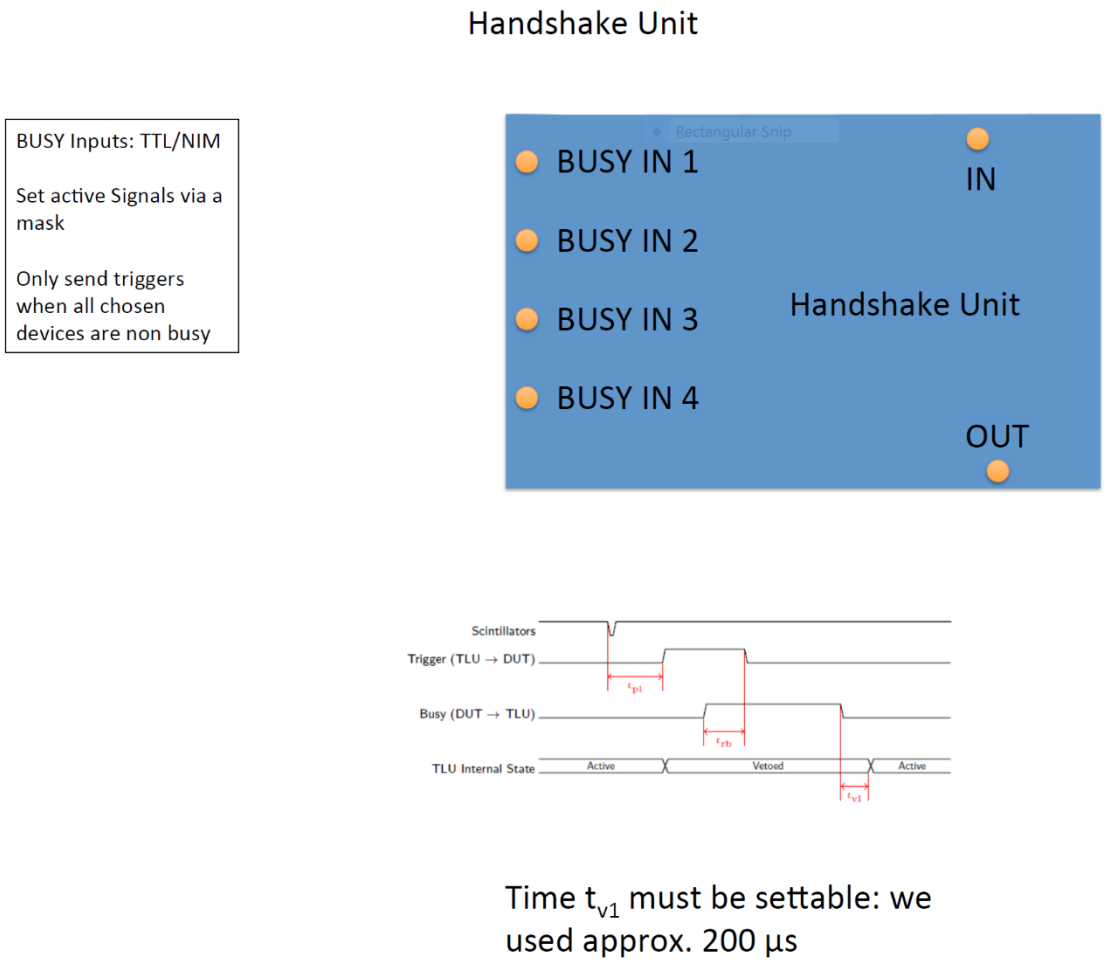


Figure 4: Original handshake unit specification

As part of choosing to use a Xilinx FPGA, we chose to use their FPGA development suite: Xilinx Vivado. This software allowed us to develop the VHDL [22] for the system, the simulations for the system, and the software for the soft-core microprocessor in the system as well as to write the firmware to the FPGA.

3.3 Interface Board

To bring the FPGA board together with the necessary inputs and outputs defined by the trigger logic, a mezzanine board needed to be designed. The mezzanine board needed to support 30 inputs and outputs for just the trigger logic going to and from the experiment. In addition to that, a 32 bit bidirectional bus was decided upon to interface with a National Instruments 9403 Bidirectional I/O Module. This interface was designed to be used for configuring the system and providing a limited data readout ability.

The board needed to connect to the Xilinx AC701 via the FMC connector and when combined with the board needed to fit with all power supplies within a 2U rack mount box. Power for the interface board was determined to be a dual supply, 15V power supply that would allow us to provide regulated power planes on the interface board of 5V and less. In addition to that power supply, the Xilinx AC701 required a separate power supply that came packaged with it.

4. Initial Implementation

The first implementation of the system started with the development of the interface board in conjunction with the high-level system of the trigger logic. First, all pins for necessary functions for the experiment were defined followed by the pins needed for the 32 bit configuration interface. Once that definition was completed, starting with the FMC connector, a board was designed.

4.1 Interface Board

The interface board was designed with every necessary connector for signals. The input and output levels were defined by the trigger logic specifications in Figure 2. The connectors for each port were defined by the specification and by requirements of the other equipment in the experiment. However, despite the various logic levels at the terminating end, the FPGA sends and receives only LVDS and LVCMOS25 signals to the interface board. This means that any input that was not strictly LVDS or LVCMOS25 required a logic converter on the board. Additionally, all LVDS inputs and outputs required onboard repeaters to provide enough driving power to drive the signals to the FPGA and to drive external outputs. The schematics for the board can be seen in Appendix A.

The TTL outputs required a LVDS-to-TTL converter chip. Then, the NIM logic converters used the same LVDS-to-TTL converter chip to go to a TTL-to-NECL converter before the signal goes into a pair of BJT transistors that provide the appropriate 600 mV, 1 ns rise time, 50 Ω impedance output signal.

After the schematic capture was completed, the board was laid out according to industry best practices to ensure the proper impedances of the traces and to ensure that

excess capacitance was not added due to the layout of the traces. Additionally, differential pairs were used to reduce the common mode noise on differential traces.

Several power planes were added to the interface board: 5V, 3.3V, 2.5V, ground, and -5V. The power planes provided low impedance paths for noise to go to ground as well as shielding traces from other layers. After the board's layout was completed, it was sent to Advanced Circuits [23] for manufacturing and once received, it was hand assembled.

4.2 Testing and Problems Uncovered

During the early testing of the prototype trigger system, several key flaws in the design of the interface board were discovered. Due to an issue with excess capacitance on the output pins of the bidirectional level shifters in the any-level discriminators and the 32-bit configuration interface, the bidirectional chips had to be removed.

Replacing the bidirectional level shifters on the any-level discriminators was accomplished by using two 1 kΩ resistors as a voltage divider (shown in Figure 5). For fixing the 32-bit interface, a mezzanine card was developed to create two 16 bit buses, one going to the FPGA and one going to the NI 9403. This change allowed testing of the remainder of the system to continue. After the first week of testing after resolving these issues, all other hardware functionality on the interface board was confirmed to work as designed.

During this testing phase, many changes to the VHDL implementation were made to ensure that the trigger system would comply with the requirements of the logic diagram.

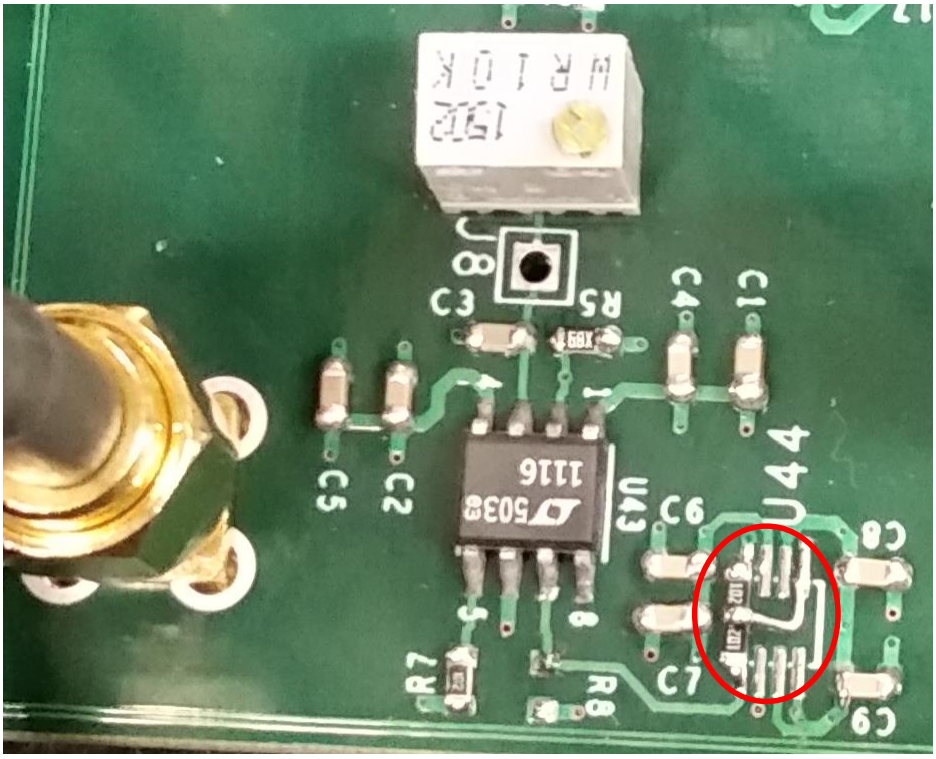


Figure 5: Image of the haywire level shifter replacing a bidirectional level-shifter in the any-level discriminator circuit.

5. Updated System Requirements and the First Field Test

After the basic functionality of the trigger system's hardware was confirmed, a decision was made to remove the problematic 32-bit interface to the NI 9403 and to replace it with an Ethernet port. Implementing Ethernet on the system was made possible using the soft microprocessor core from Xilinx, MicroBlaze [24]. The system's implementation of the MicroBlaze ran a HTTP [25] server using lwIP [26], a lightweight TCP/IP [27] stack. It communicated with the trigger logic through an AXI bus which had access to every configuration register and counter register in the trigger logic.

To interface with the HTTP server running on the trigger system, a graphical user interface was written using Qt and C++ for use on Linux systems. The program has the ability to readout every register in the trigger unit, and to reset and configure the entire trigger system.

After the switch to the Ethernet communication system was completed, the device was sent to the Paul Scherrer Institute (PSI) to be tested as part of an active experiment. At the experiment, it performed as specified by the trigger logic and I/O specifications. Despite this, a full test of the device's capabilities in direct comparison to those of the EUDET JRA1 TLU has not been completed. Testing to confirm that the device solves all of the issues with the EUDET JRA1 TLU will commence after the device has been updated based on feedback from the operators of the beam test at PSI.

6. Future Work

After the first beam test using this new trigger system, a number of changes were proposed by operators of the trigger system. These changes include an updated trigger logic (shown in Figure 6 and Figure 7Figure 3**Error! Reference source not found.**), a new mode of operation for the handshake unit (Figure 8), two precision clock outputs (Figure 9), and an updated static IP assignment for the trigger system.

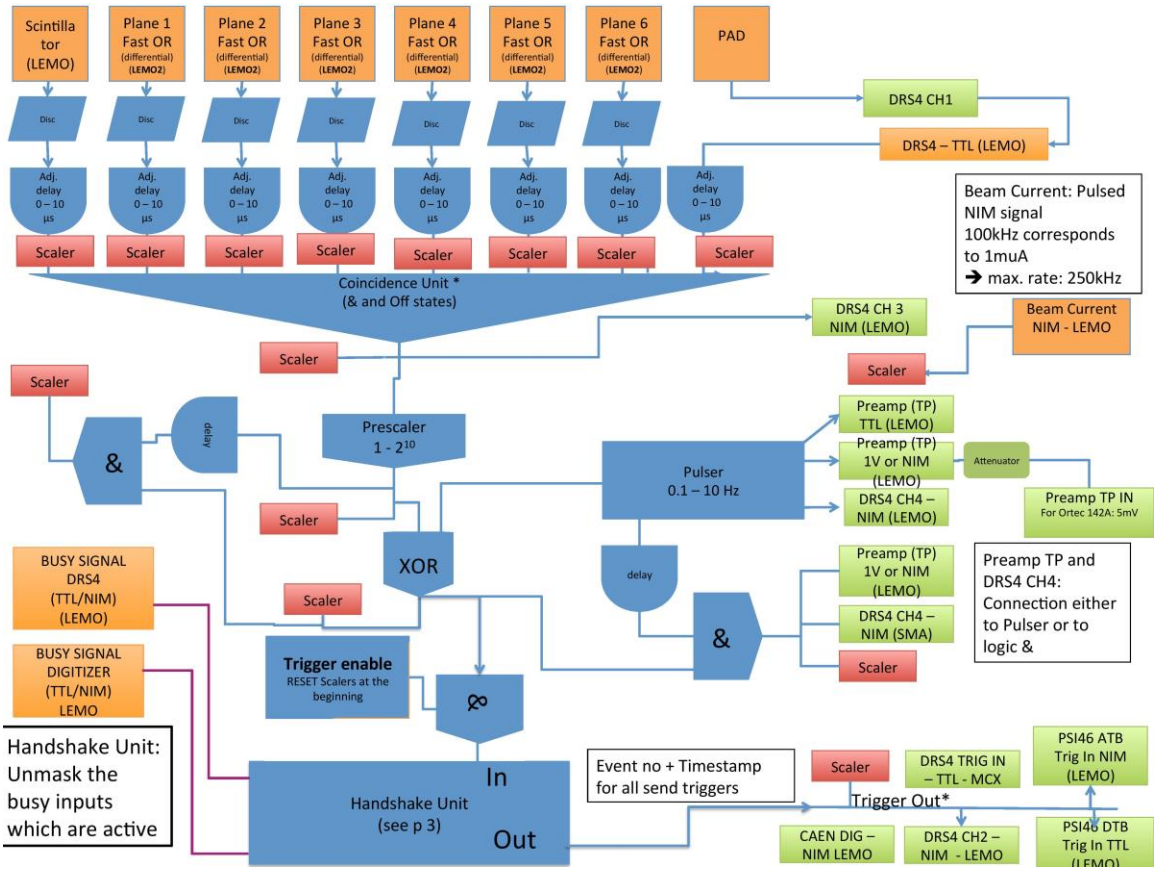


Figure 6: Updated trigger logic

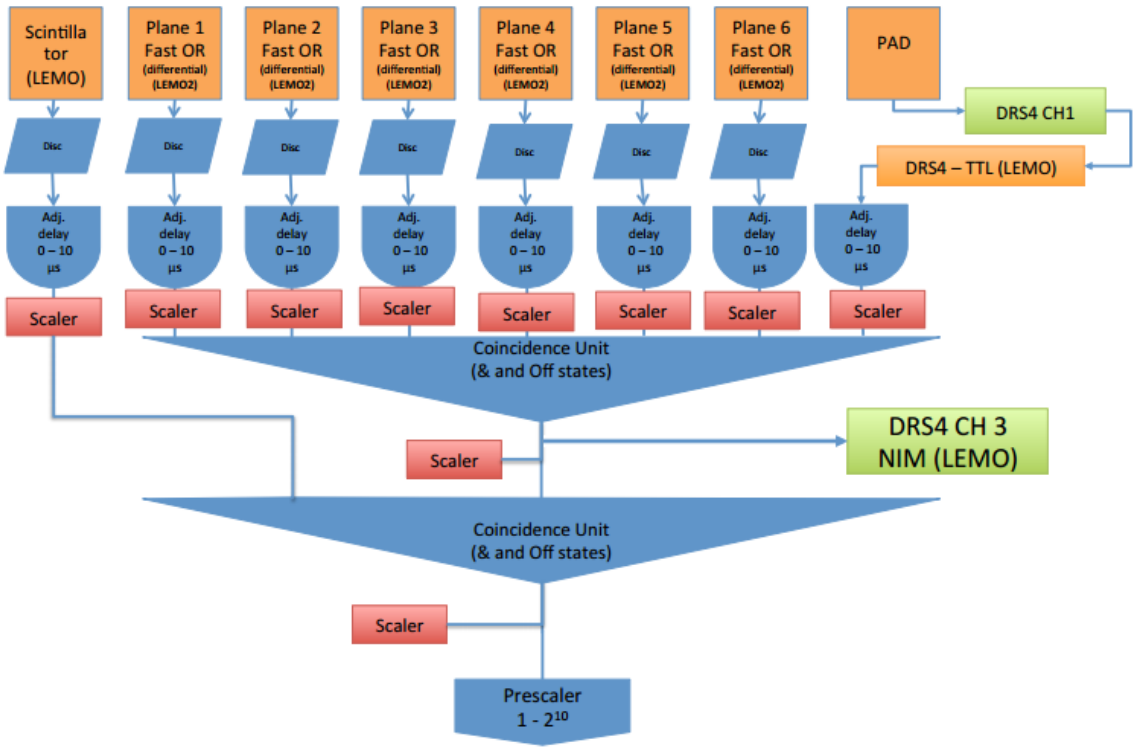


Figure 7: Updated coincidence unit logic

The updated trigger logic contains a few changes primarily in relation to coincidence unit (although a few small changes were made to output specifications). Additionally, the scalers in the coincidence unit and front-end delays will be changed from 16 to 32 bits to avoid integer overflow during a run. Finally, DRS4 CH3 will be moved from the output of the second stage of the coincidence unit to the output of the first stage of the coincidence unit (change not shown in drawings).

The update to the handshake is the request for a mode where not all BUSY signals must be low (not busy) before sending the output triggers. This will allow for independent handshakes for each trigger rather than a single handshake for every trigger. The operators

should be able to switch between modes during runtime to achieve their desired data collection method.

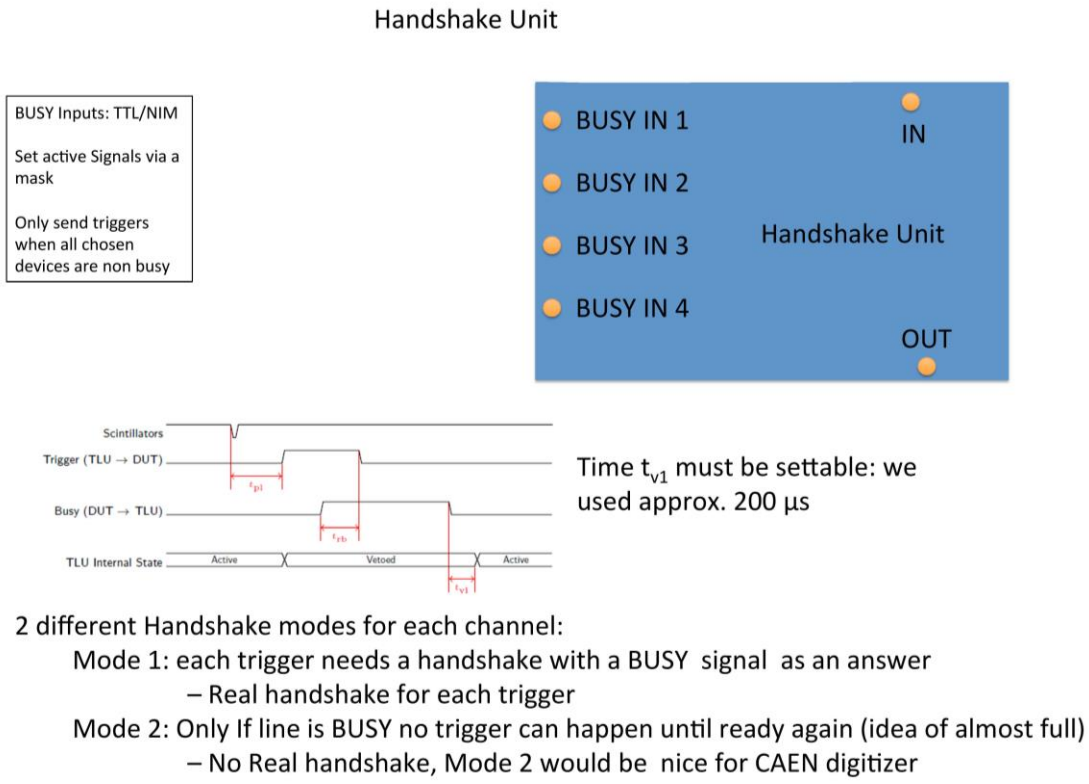


Figure 8: Updated behavior for the handshake unit

The last currently proposed change is the addition of two TTL clock outputs to the experiment. This would allow all devices in the experiment to be tied together through a common clock tree to decrease the possibility of race conditions when different devices are interacting with each other. Beyond the changes already proposed by the operators of the system, several other changes may occur over time such as the creation of a new, fixed interface board and case that is designed to correct the haywires needed on the first board and to replace the 32-bit interface with additional unused I/O ports to allow for continued development of the trigger system's functionality.

External Clock DTB (New 28/8/2015)

When running with multiple Digital Testboards an external clock (40MHz) must be provided

The testboards might need different phases wrt to each other:
Signals: TTL

Would be great to have
two 40Mhz TTL outputs (LEMO) where the phase can be changed in
1 ns steps wrt each other (25 settings)

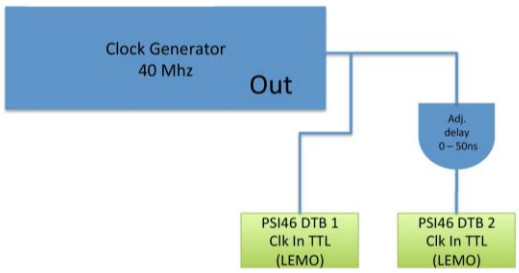


Figure 9: Logic requirements for precision clock outputs

7. References

[1] CERN, "LHC Season 2 facts & figures," http://press.web.cern.ch, 2013.

[2] L. Evans and P. Bryant, "LHC Machine," *Journal of Instrumentation,* vol. 3, no. August 2008, 2008.

[3] M. Mathes, M. Cristinziani, H. Kagan, S. Smith, W. Trischuk, J. Velthius and N. Wermes, "Characterization of a single crystal diamond pixel detector in a high energy particle beam," *Journal of Instrumentation,* vol. 3, p. P12002, 2008.

[4] S. Zhao, "Characterization of the Electrical Properties of Polycrystalline Diamond Films," 1994.

[5] Paul Scherrer Institute, "The Paul Scherrer Institute in brief," [Online]. Available: https://www.psi.ch/about/psi-in-brief. [Accessed November 2015].

[6] Paul Scherrer Institute, "Swiss Light Source," Paul Scherrer Institute, 2012.

[7] J. Treis, P. Fischer, H. Krüger, L. Klingbeil, T. Lari and N. Wermes, "A modular PC based," *Nuclear Instruments,* vol. 490, pp. 112-123, 2002.

[8] *Final Report - Detector Research and Development towards the International Linear Collider,* DESY, 2011.

[9] D. Cussans, *Description of the JRA1 Trigger Logic Unit (TLU), v0.2c,* EUDET, 2009.

[10] "The International Linear Collider: Technical Desiged Report," International Linear Collider, 2013.

[11] TIA, "ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTERFACE CIRCUITS," 2000.

[12] J. L. Buie, "Coupling transistor logic and other circuits". United State of America Patent 3283170, 8 September 1961.

[13] ORTEC, *Electronics Standards and Definitions*, ORTEC.

[14] University of Bristol, "Particle Physics," University of Bristol School of Physics, 2015. [Online]. Available: http://www.bristol.ac.uk/physics/research/particle/.

[15] ETH Zurich, "Institute for Particle Physics," ETH Zurich Department of Physics, 2015. [Online]. Available: http://www.ipp.phys.ethz.ch/.

[16] K. Gabathuler, *PSI46 Pixel Chip - External Specification*, Villigen, Switzerland: Paul Scherrer Institute, 2004.

[17] Paul Scherrer Institute, *DRS4 - 9 Channel, 5 GSPS Switched Capacitor Array*, Paul Scherrer Institute, 2009.

[18] "Xilinx," Xilinx, 2015. [Online]. Available: http://www.xilinx.com/.

[19] Xilinx, *Spartan-6 Family Overview*, Xilinx, 2011.

[20] Xilinx, *AC701 Evaluation Board for the Artix-7 FPGA*, Xilinx, 2015.

[21] Xilinx, *XA Artix-7 FPGAs Overview*, Xilinx, 2014.

[22] Design Automation Standards Committee, *IEEE Standard VHDL Language Reference Manual*, New York, NY: IEEE, 2009.

[23] "Advanced Circuits," Advanced Circuits, 2015. [Online]. Available: http://www.4pcb.com/.

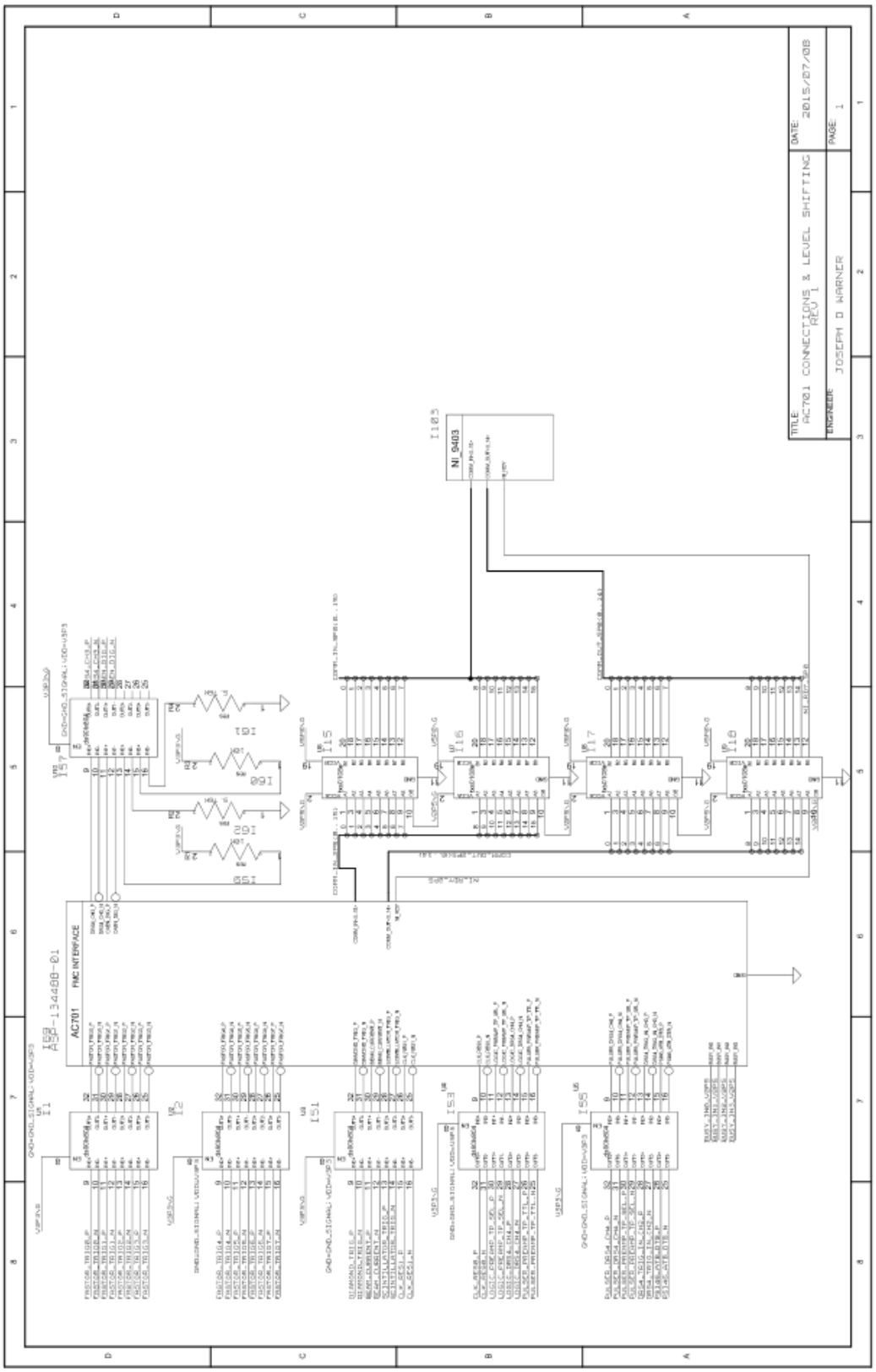
[24] Xilinx, *MicroBlaze Processor Reference Guide Embedded Development Kit EDK 11.4,* Xilinx, 2009.

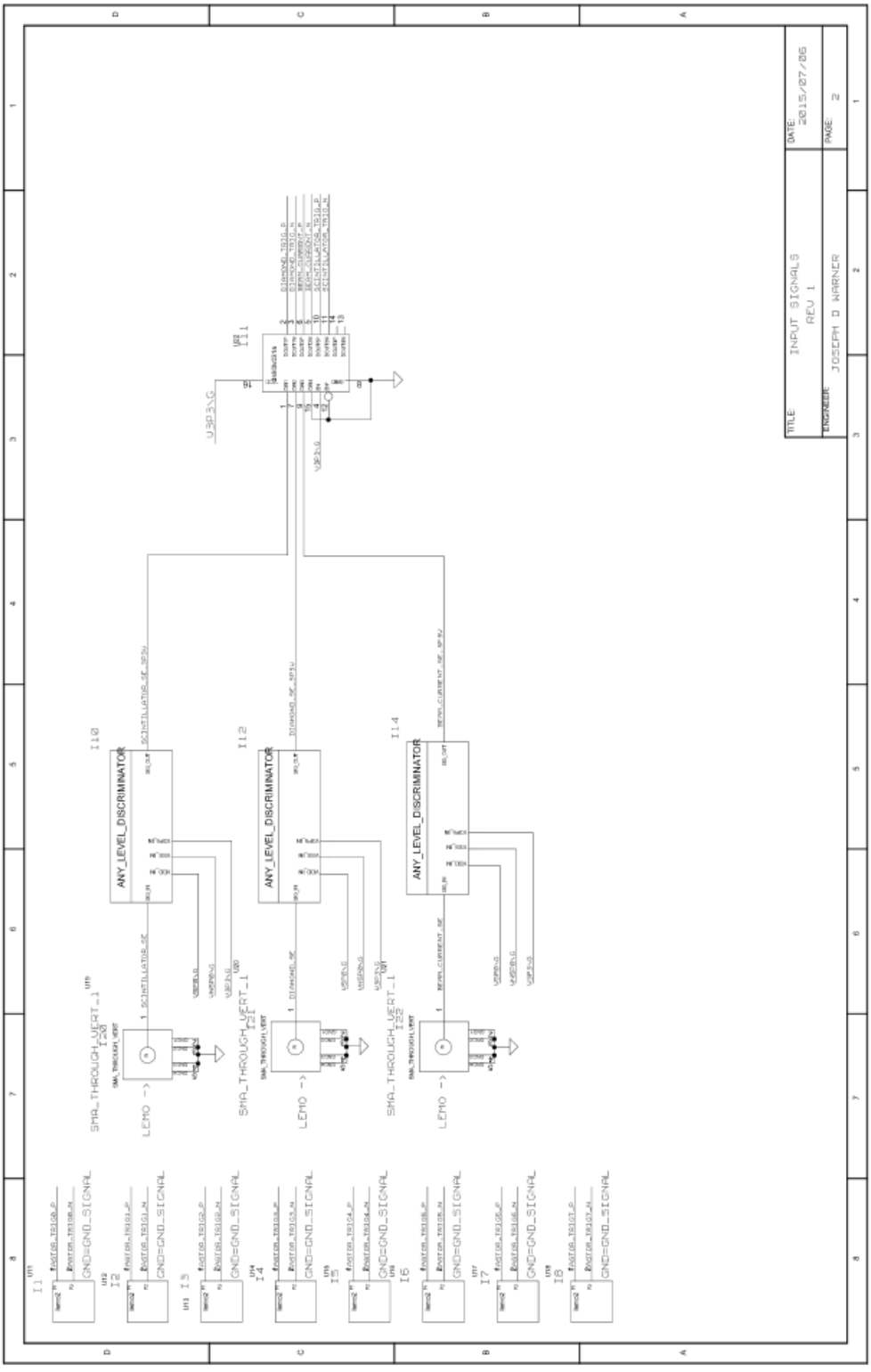
[25] Network Working Group, *Hypertext Transfer Protocol -- HTTP/1.1,* IETF, 1999.

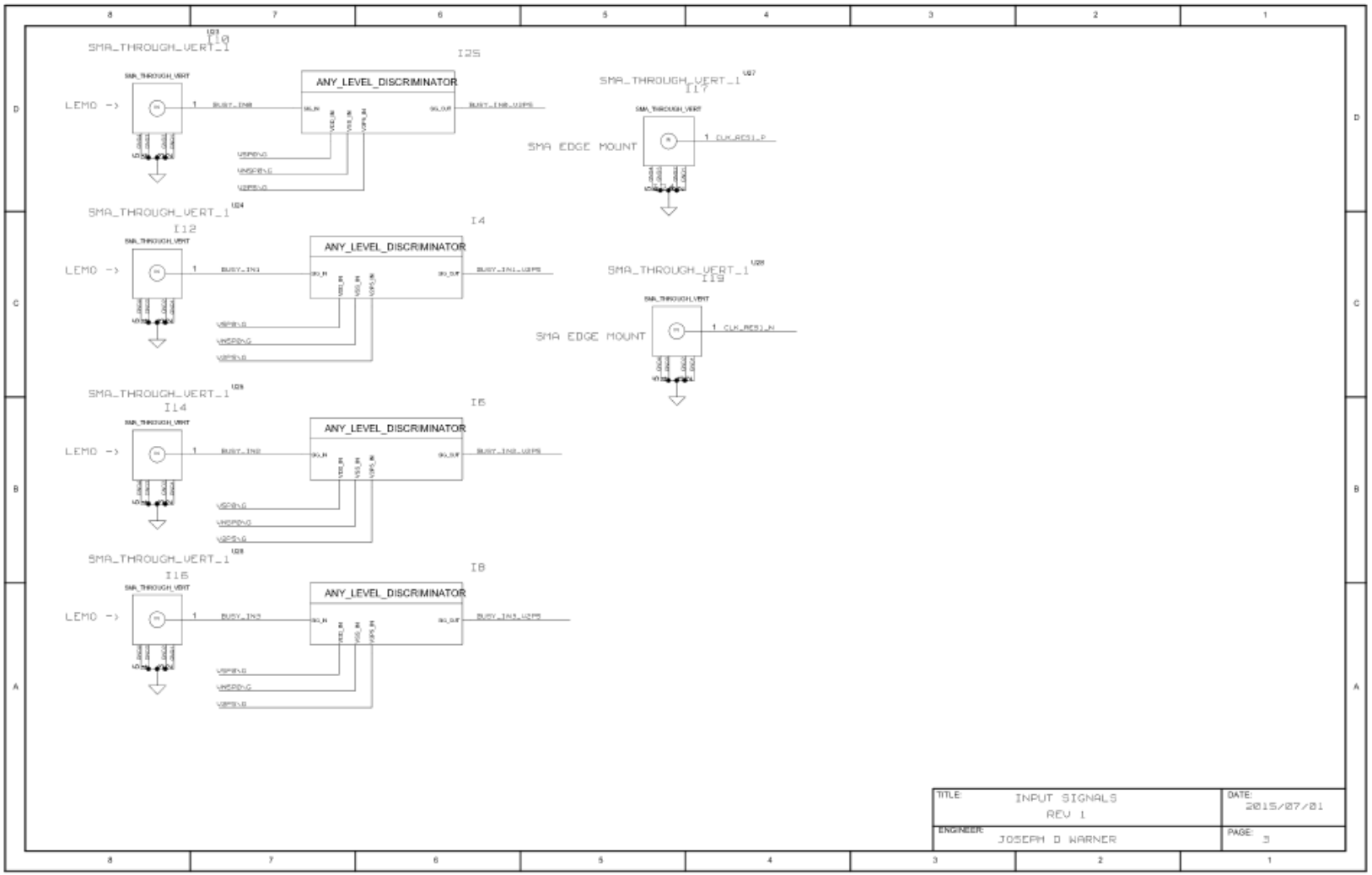
[26] "lwIP - A Lightweight TCP/IP stack - Summary," Free Software Foundation, 2015. [Online]. Available: http://savannah.nongnu.org/projects/lwip/.

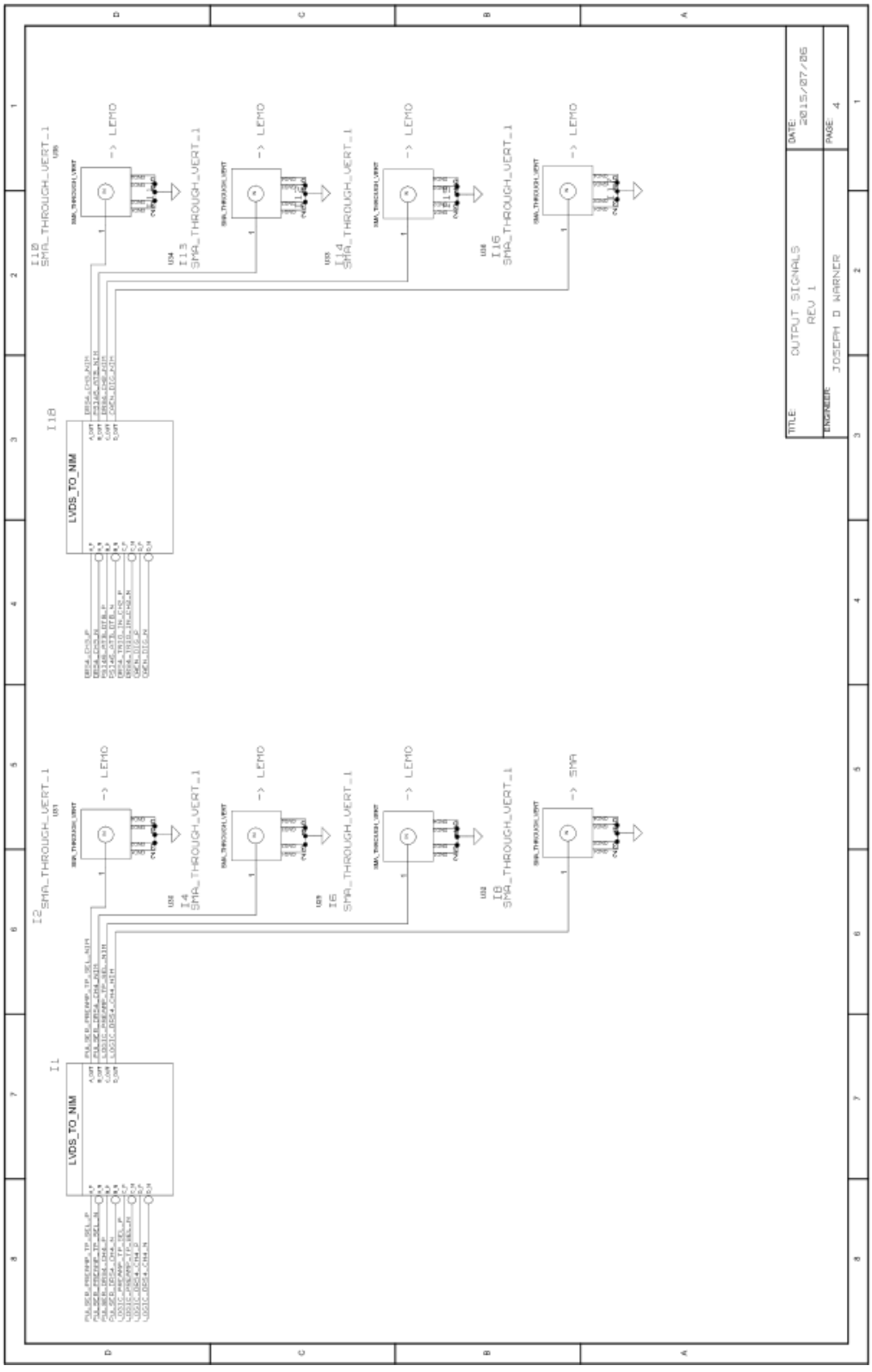
[27] V. Cerf and Y. Dalal, *Specification of Internet Transmission Control Program,* IETF, 1974.

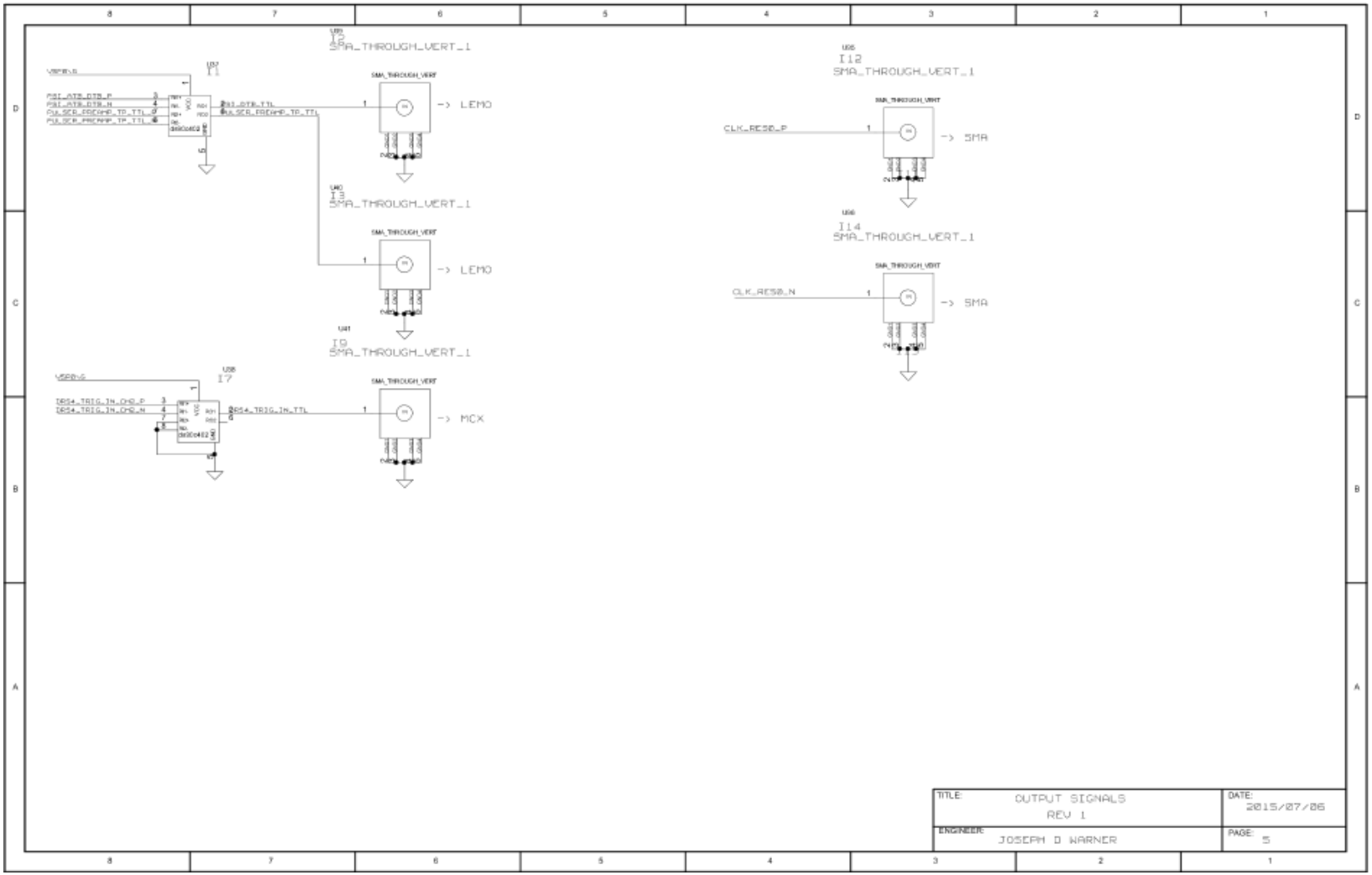
Appendix A: Trigger Unit PCB Schematic

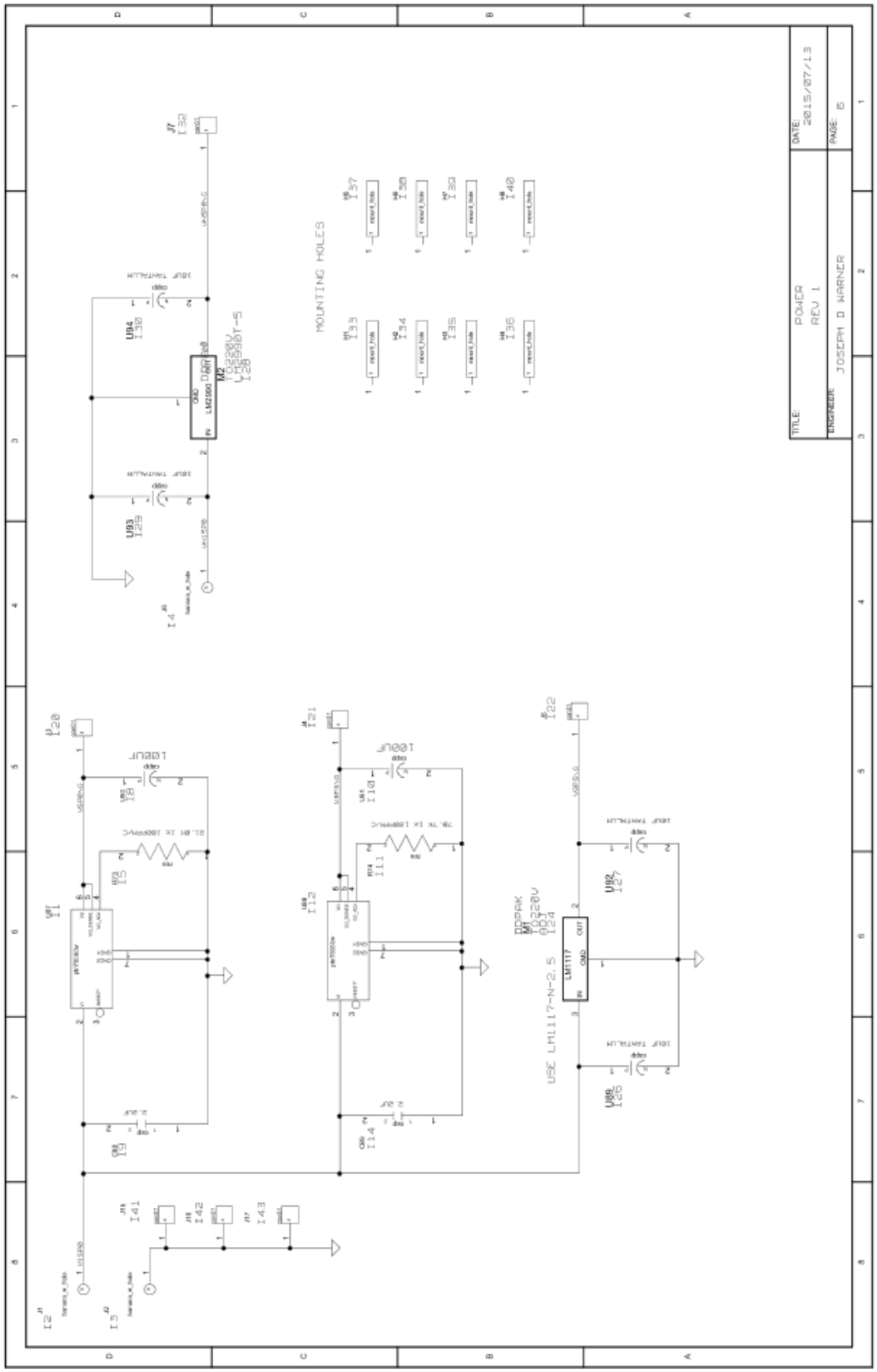

AC701 CONNECTIONS & LEVEL SHIFTING
REV 1
JOSEPH D WARNER
2015/07/08
PAGE 1
AC701 FMC INTERFACE
NI_9403

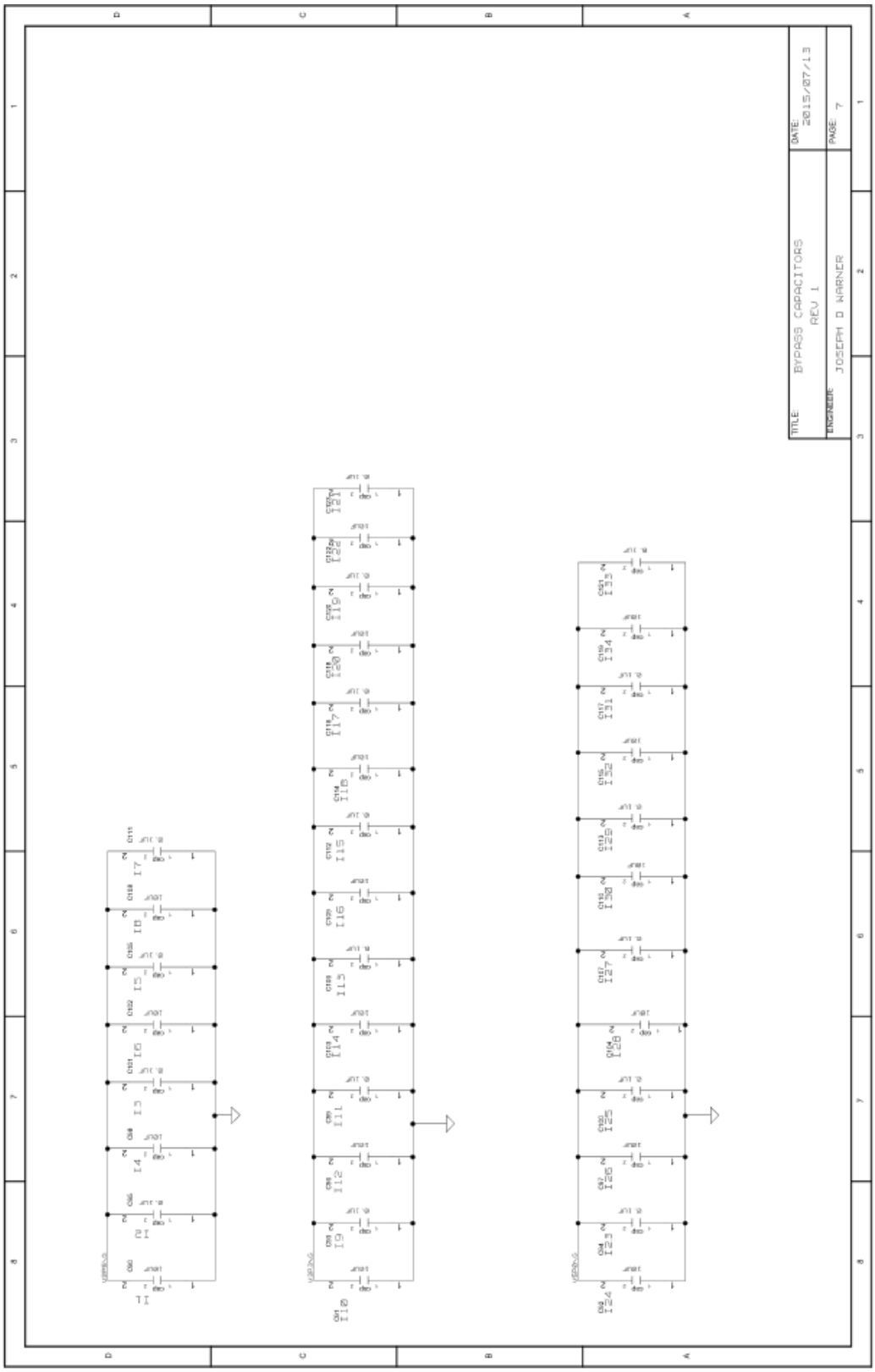

TITLE: INPUT SIGNALS
REV 1
DATE: 2015/07/06
ENGINEER: JOSEPH D WARNER
PAGE: 2
ANY_LEVEL_DISCRIMINATOR
SMA_THROUGH_VERT_1
LEMO ->
GND=GND_SIGNAL

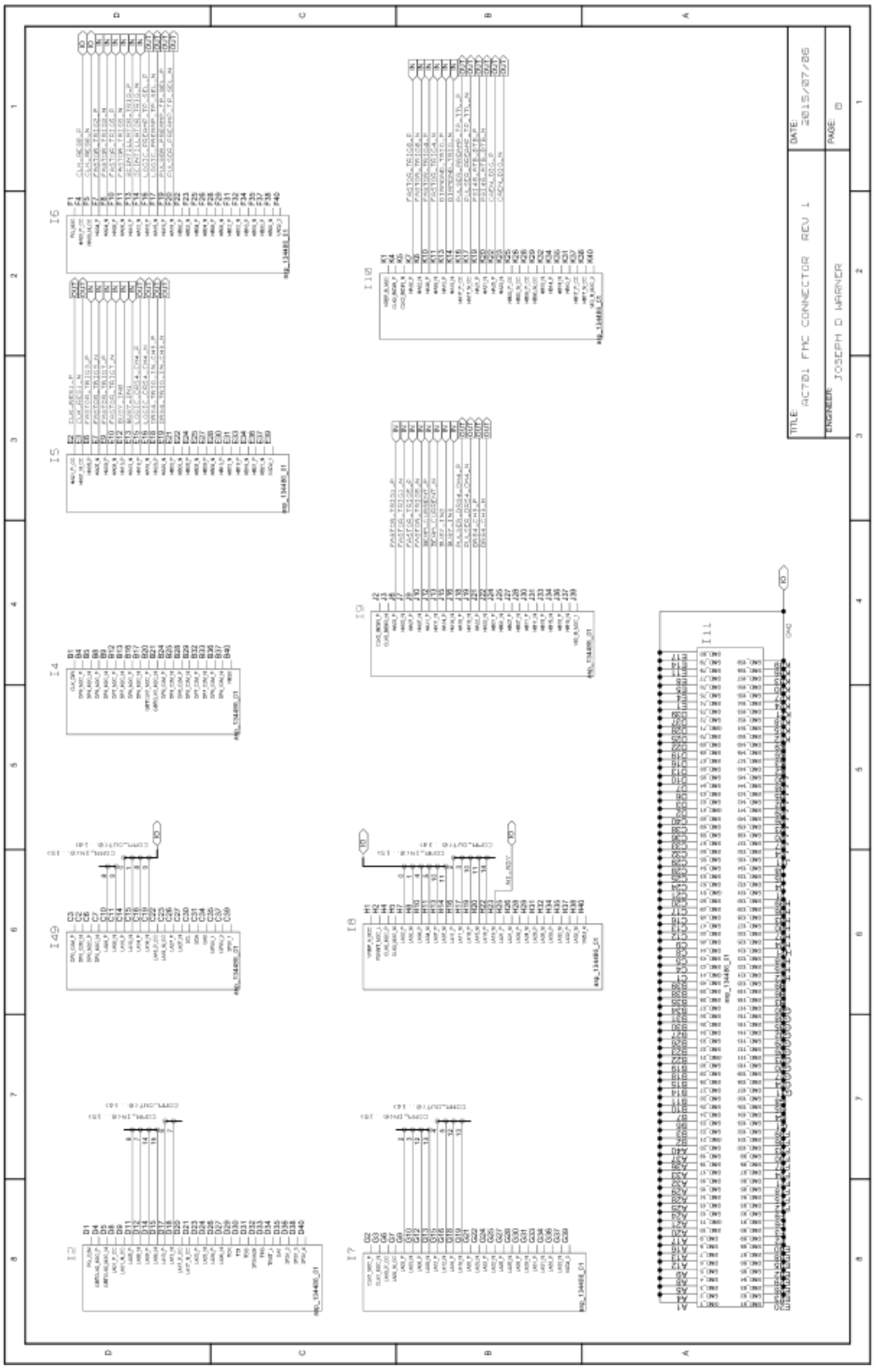

SMA_THROUGH_VERT_1
I10
I25
ANY_LEVEL_DISCRIMINATOR
LEMO ->
SMA_THROUGH_VERT_1
I17
SMA EDGE MOUNT
SMA_THROUGH_VERT_1
I12
I4
ANY_LEVEL_DISCRIMINATOR
LEMO ->
SMA_THROUGH_VERT_1
I13
SMA EDGE MOUNT
SMA_THROUGH_VERT_1
I14
I6
ANY_LEVEL_DISCRIMINATOR
LEMO ->
SMA_THROUGH_VERT_1
I15
I8
ANY_LEVEL_DISCRIMINATOR
LEMO ->
TITLE: INPUT SIGNALS REV 1
DATE: 2015/07/01
ENGINEER: JOSEPH D WARNER
PAGE: 3

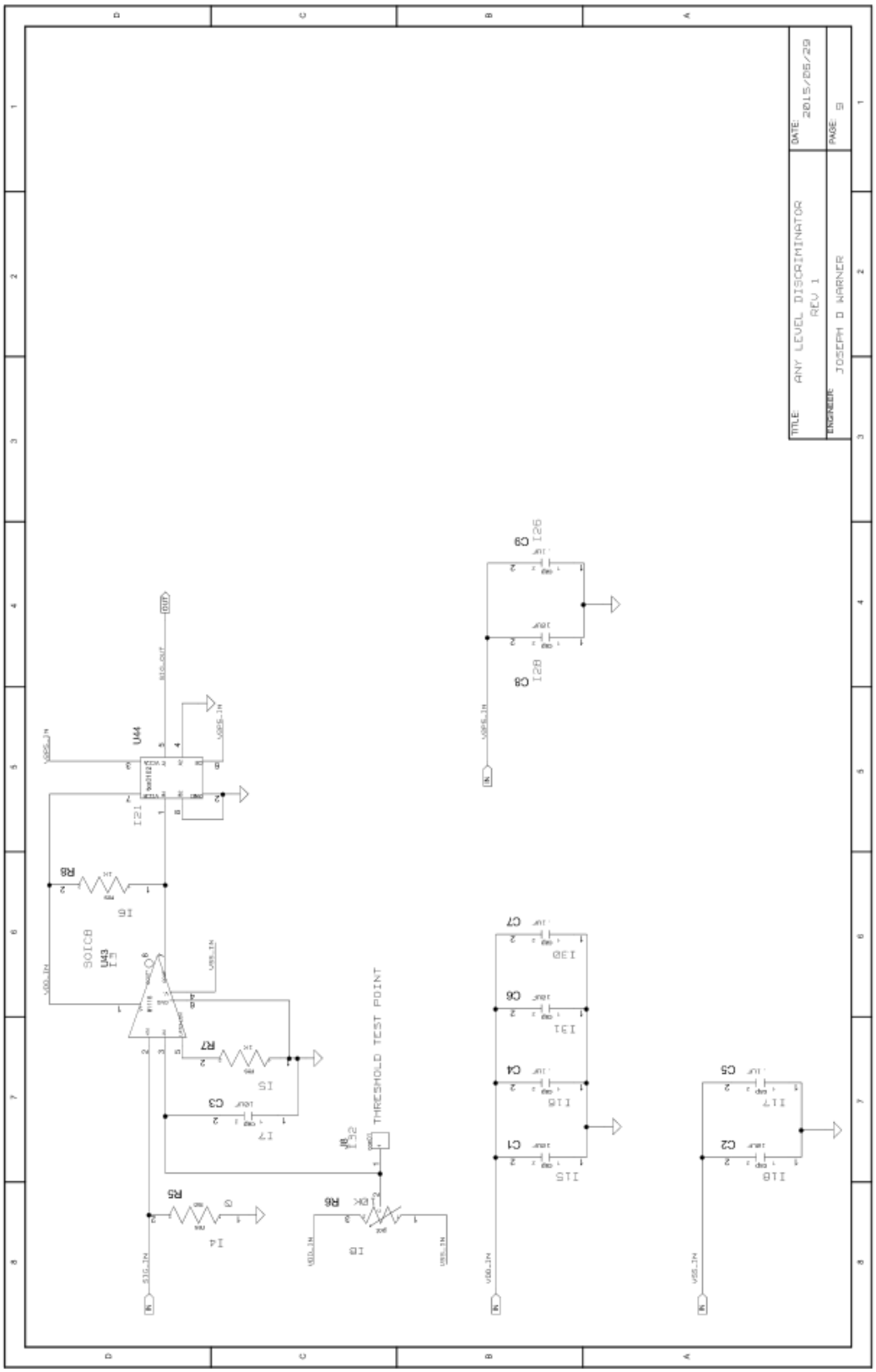

TITLE: OUTPUT SIGNALS
REV 1
DATE: 2015/07/06
ENGINEER: JOSEPH D WARNER
PAGE: 4
LVDS_TO_NIM
SMA_THROUGH_VERT_1
-> LEMO
-> SMA

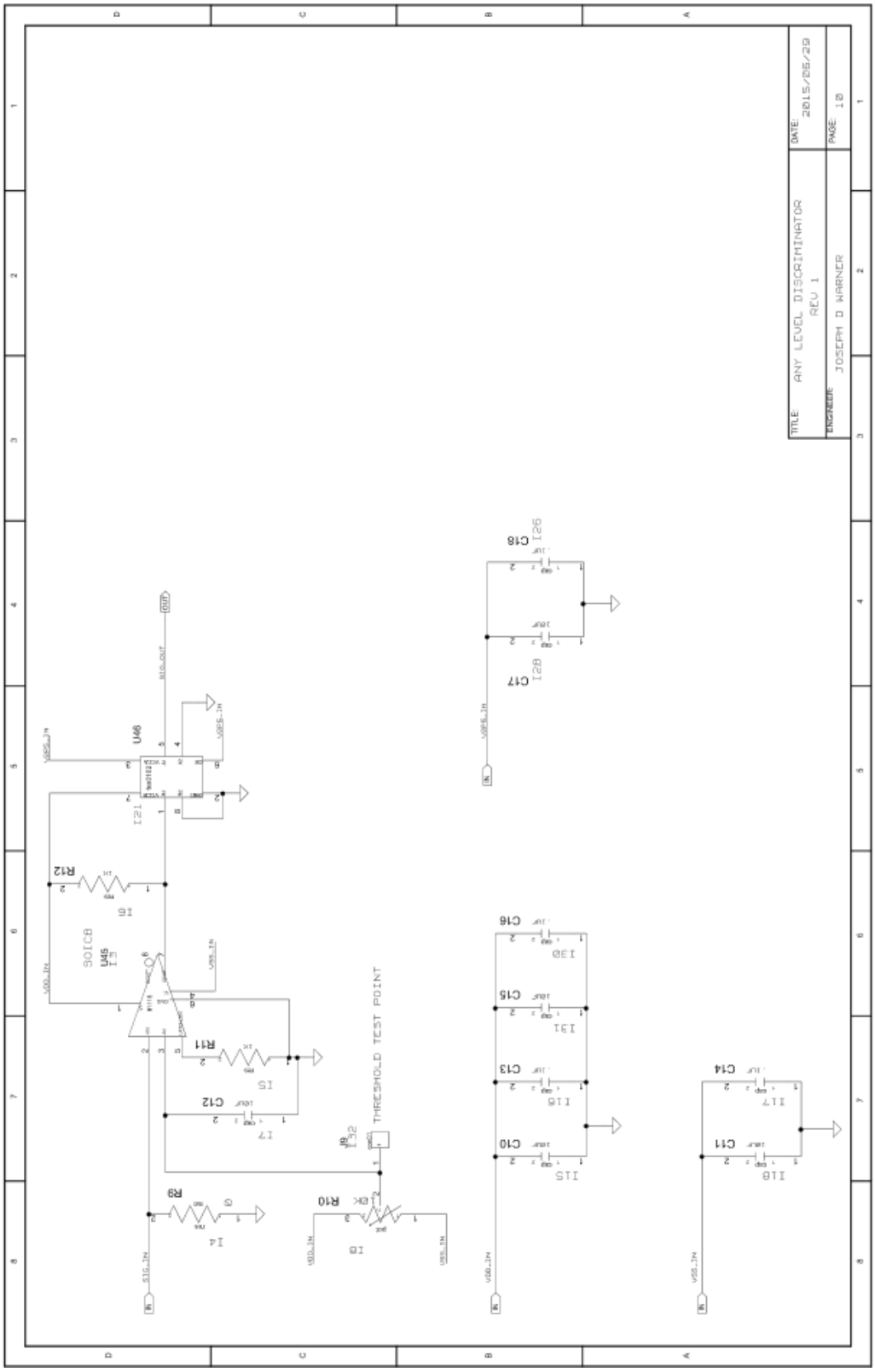

SMA_THROUGH_VERT_1
-> LEMO
-> LEMO
-> MCX
-> SMA
-> SMA
CLK_RES0_P
CLK_RES0_N
TITLE: OUTPUT SIGNALS REV 1
DATE: 2015/07/06
ENGINEER: JOSEPH D WARNER
PAGE: 5

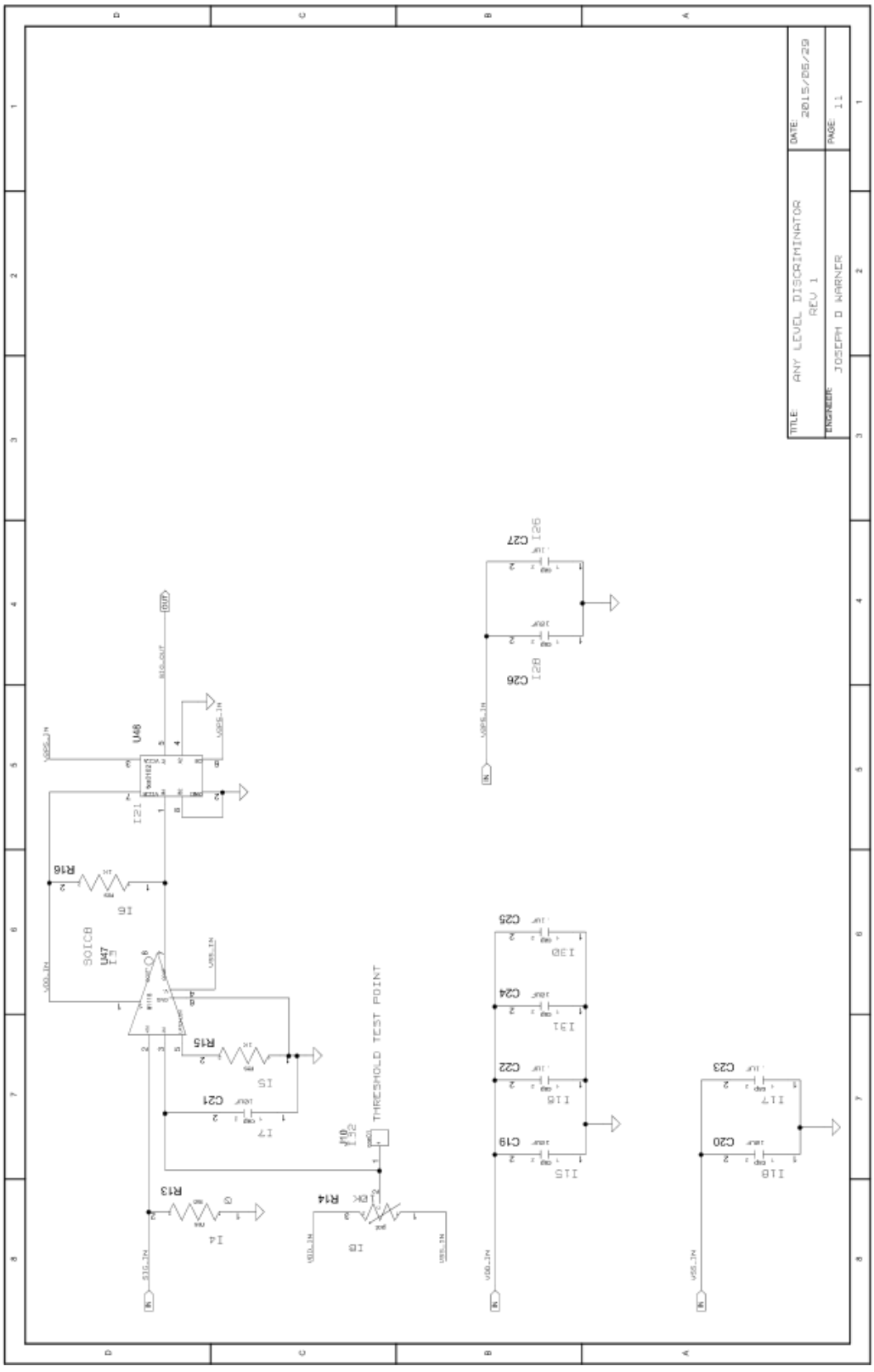

MOUNTING HOLES
LM1117-N-2.5
TITLE: POWER REV 1
DATE: 2015/07/13
ENGINEER: JOSEPH D WARNER
PAGE: 5

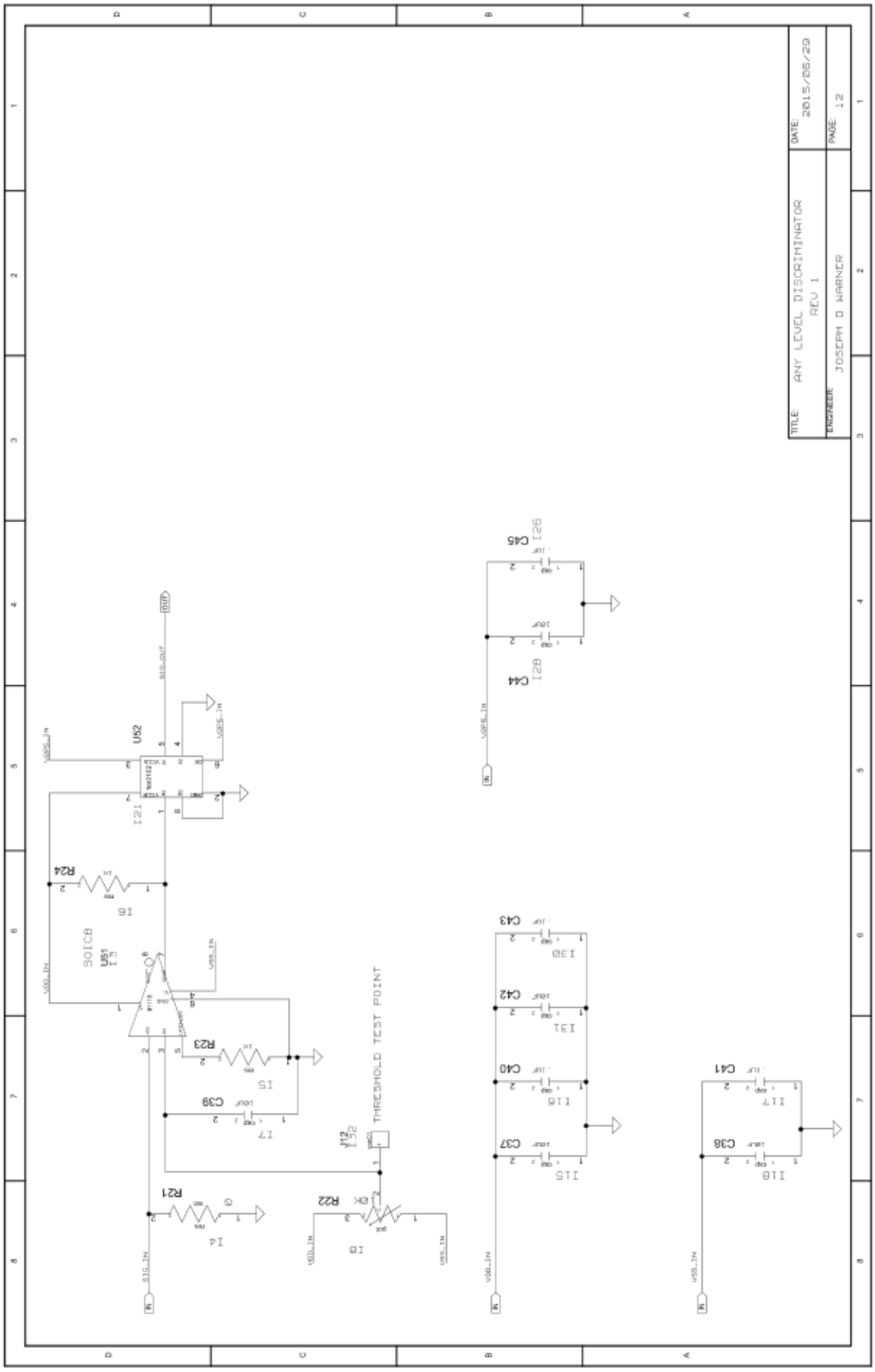

TITLE: BYPASS CAPACITORS
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/07/13
PAGE 7

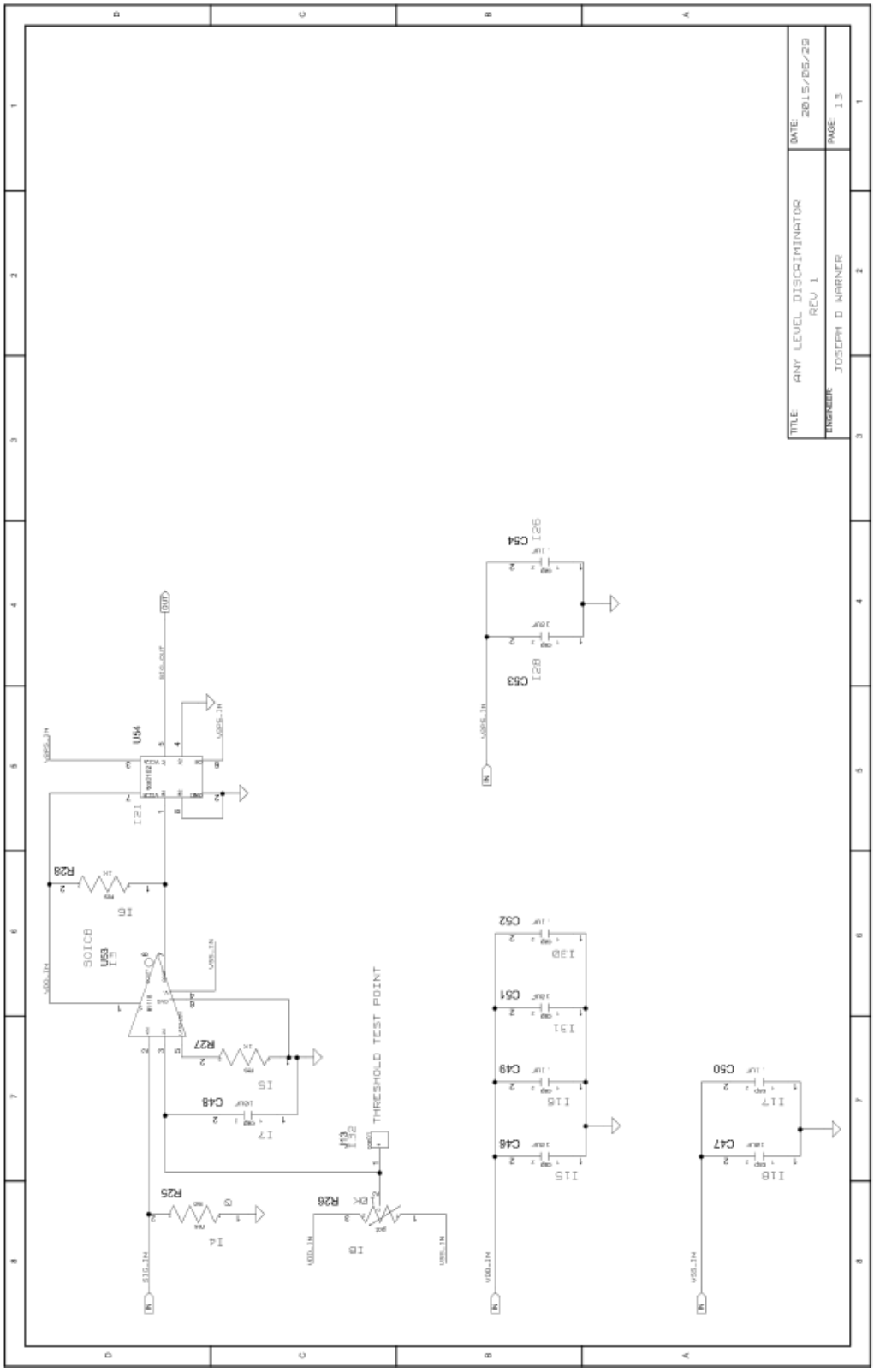

TITLE: AC701 FMC CONNECTOR REV 1
DATE: 2015/07/06
ENGINEER: JOSEPH D WARNER
PAGE: B

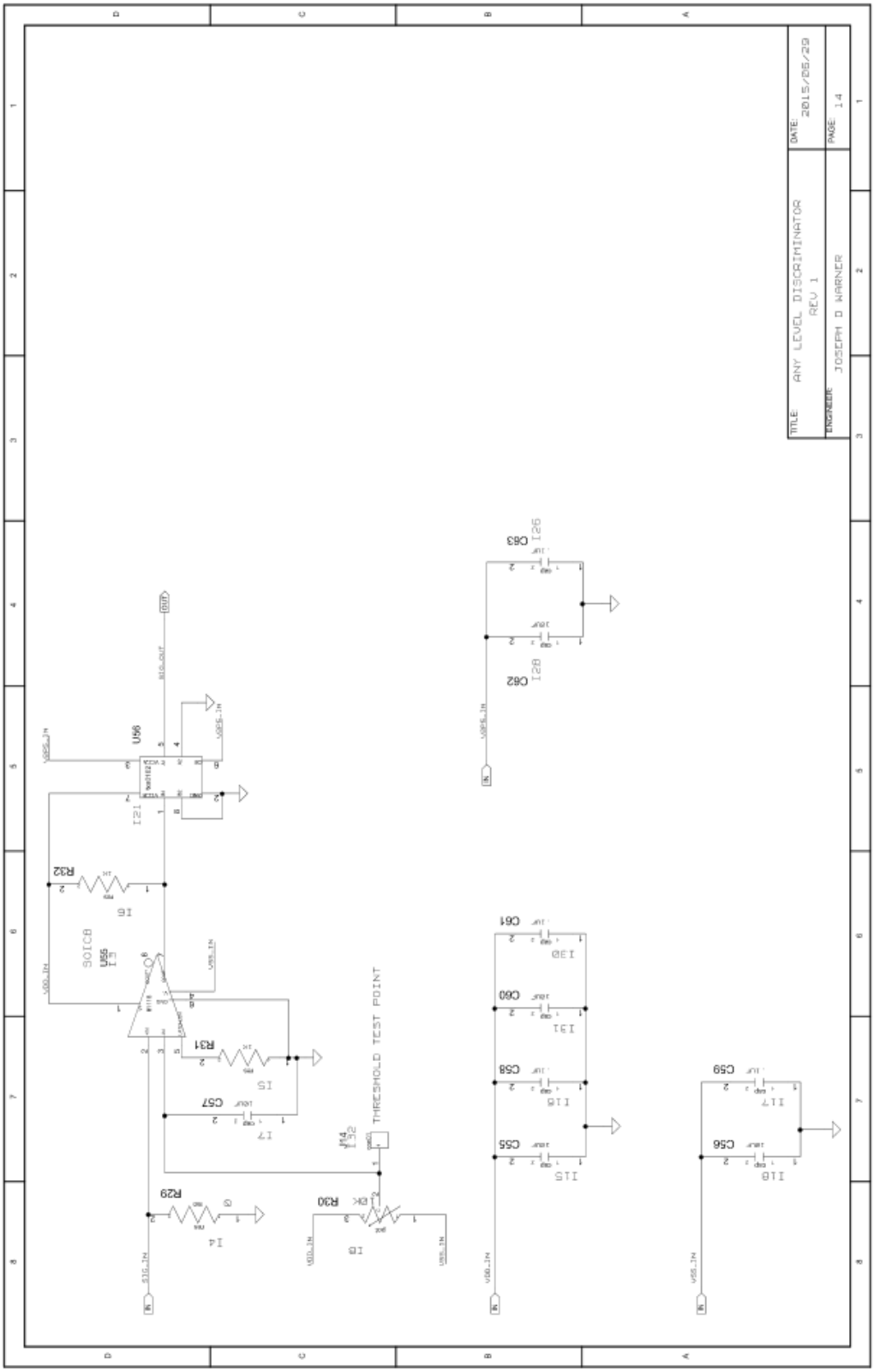

TITLE: ANY LEVEL DISCRIMINATOR
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/05/29
PAGE: 9
THRESHOLD TEST POINT
SOIC8
U44
U43
R8
R7
R6
R5
C9
C8
C7
C6
C5
C4
C3
C2
C1

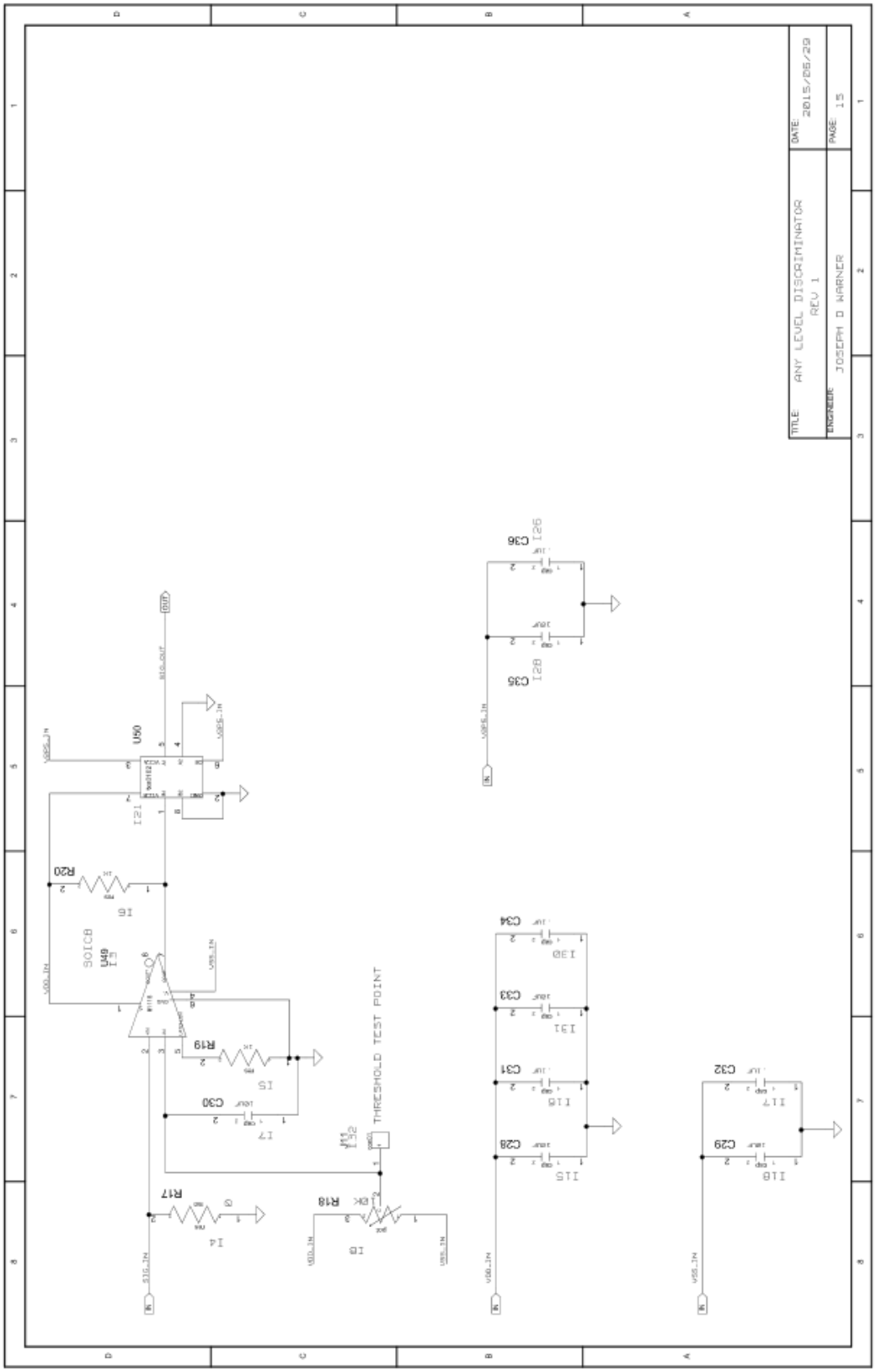

TITLE: ANY LEVEL DISCRIMINATOR
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/05/20
PAGE: 10
THRESHOLD TEST POINT
SOIC8
R12
R11
R9
R10
C12
C18
C17
C16
C15
C13
C10
C14
C11
U46
U45
VDD_IN
VSS_IN
BIG_OUT
OUT

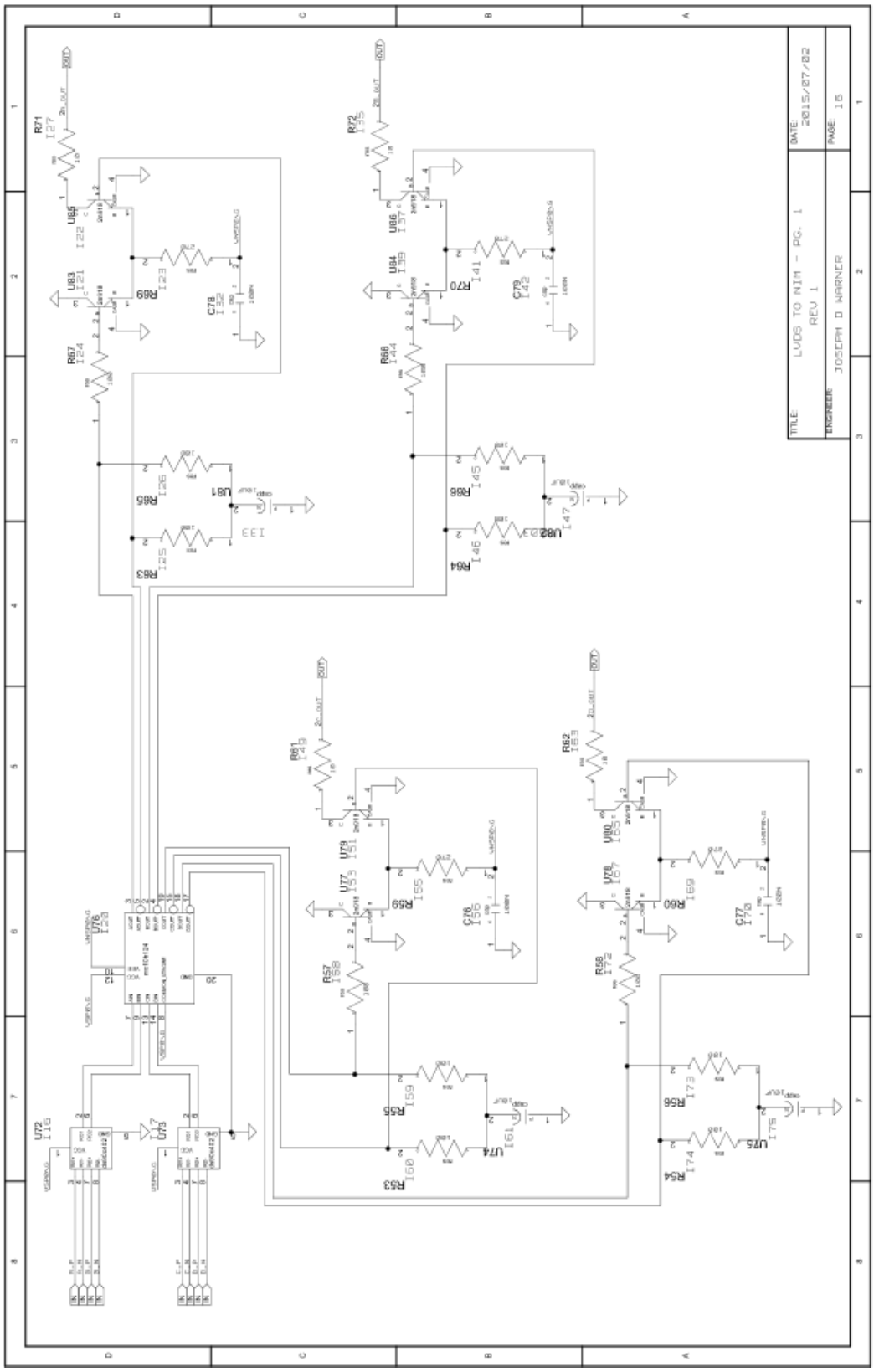

TITLE: ANY LEVEL DISCRIMINATOR
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/05/20
PAGE: 11
THRESHOLD TEST POINT
SOICB
U46
U47
R16
R15
R13
R14
C21
C27
C26
C25
C24
C22
C19
C23
C20

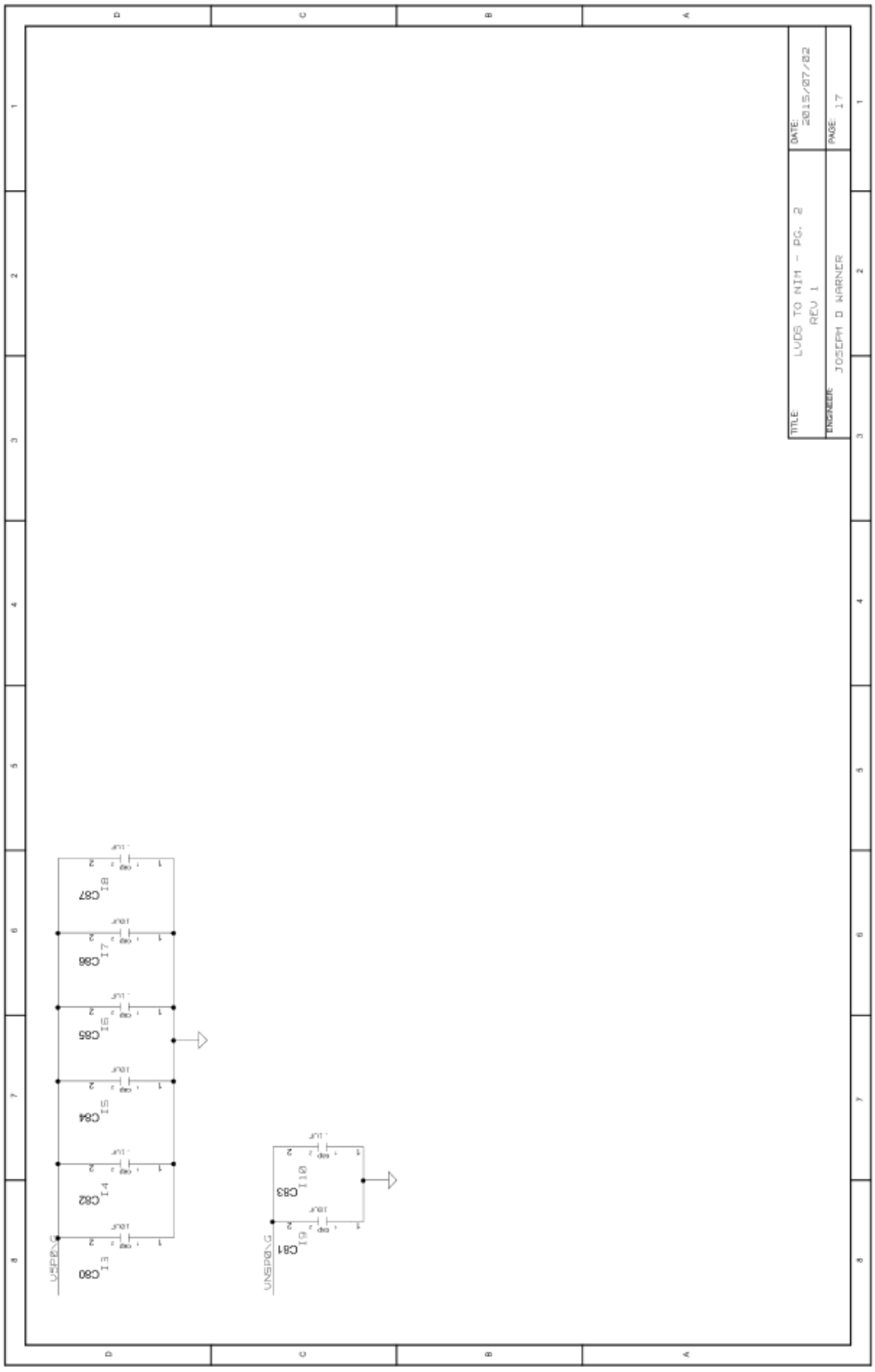

TITLE: ANY LEVEL DISCRIMINATOR
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/05/29
PAGE: 12
THRESHOLD TEST POINT
U52
U51
R24
R23
R22
R21
C39
C45
C44
C43
C42
C40
C37
C41
C38

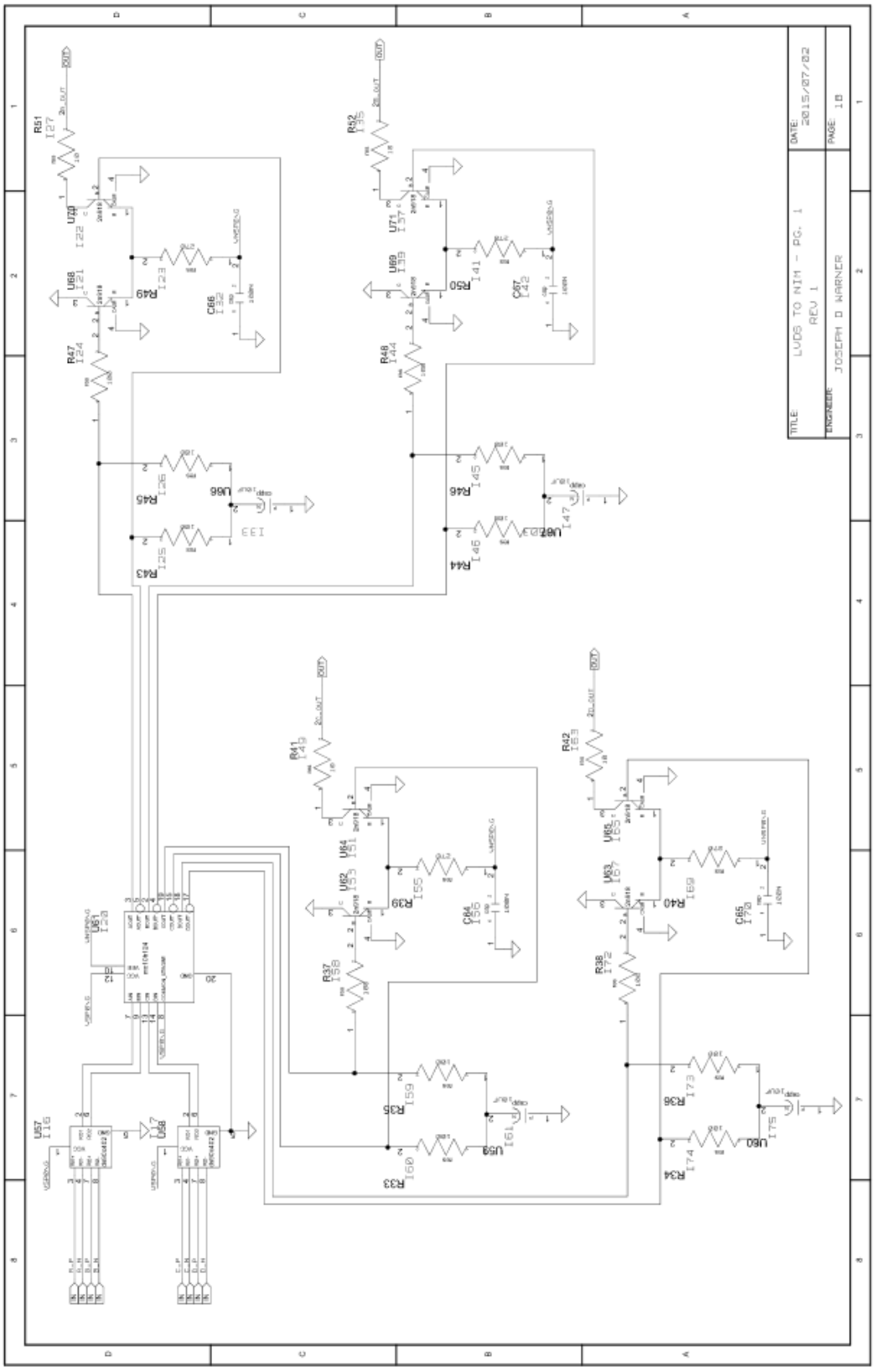

TITLE: ANY LEVEL DISCRIMINATOR
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/05/29
PAGE: 13
THRESHOLD TEST POINT
SOICB

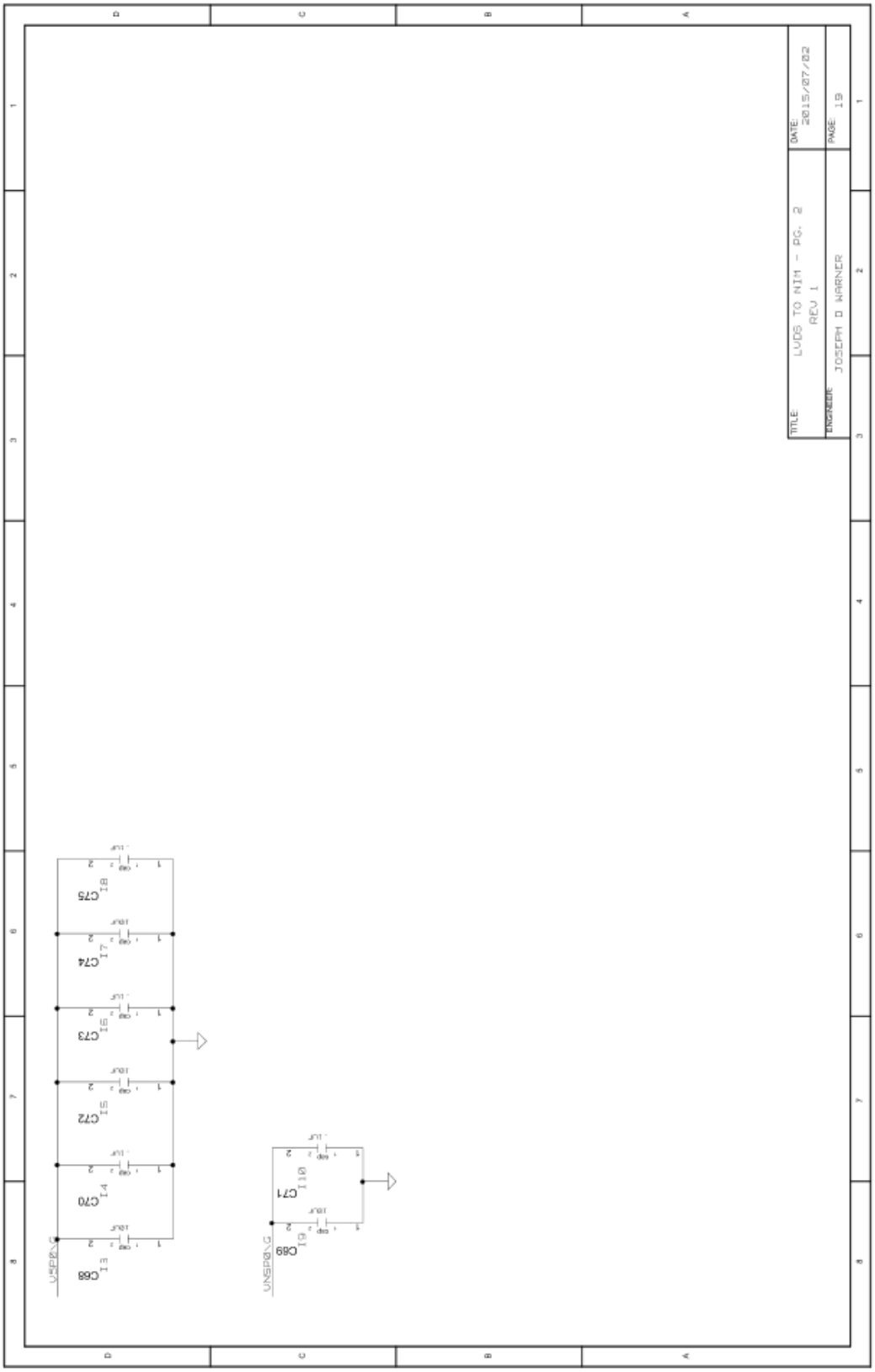

TITLE: ANY LEVEL DISCRIMINATOR
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/06/29
PAGE: 14
THRESHOLD TEST POINT
SOIC8

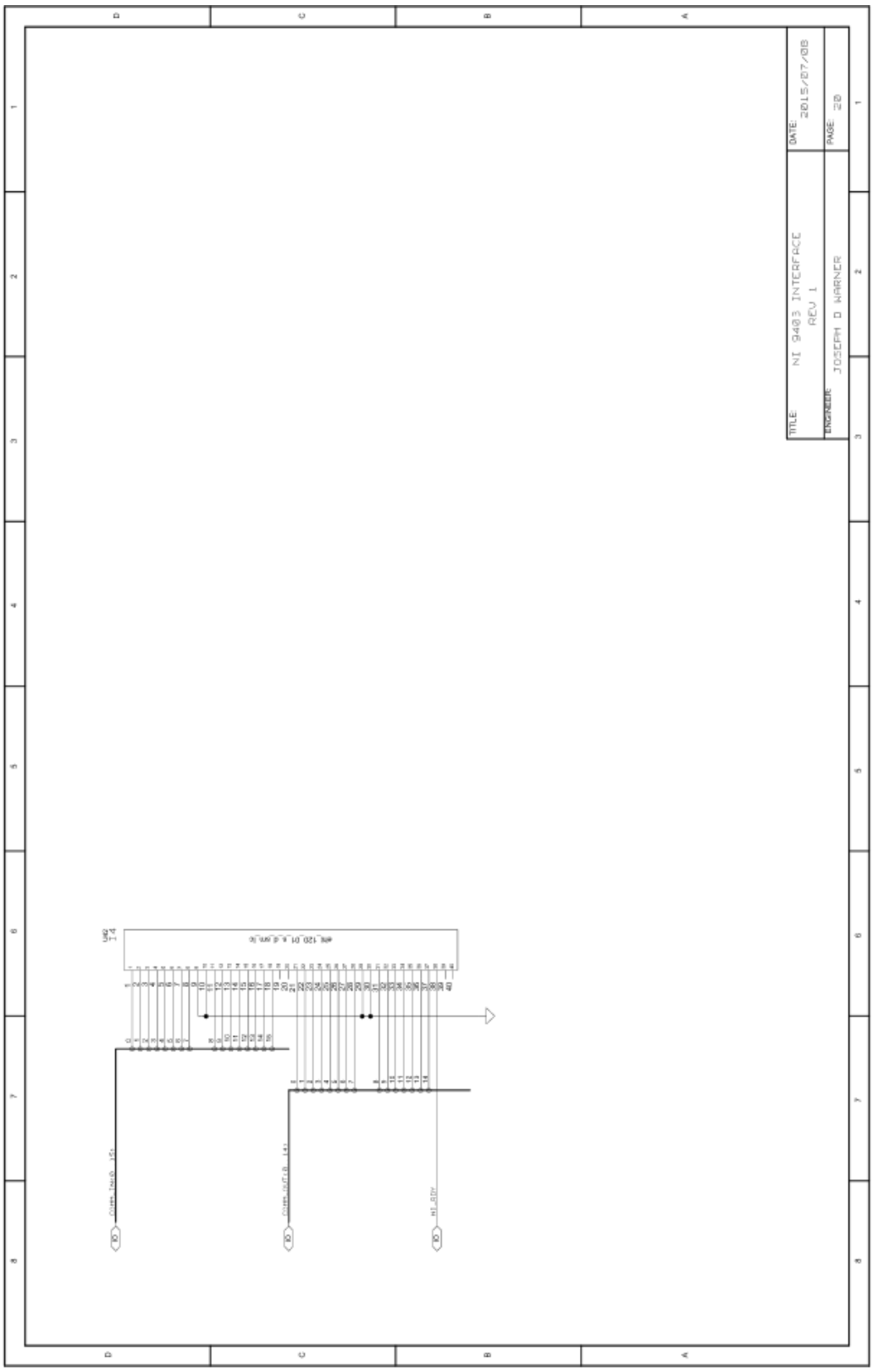

TITLE: ANY LEVEL DISCRIMINATOR
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/05/29
PAGE: 15
THRESHOLD TEST POINT
SOIC8
U49
U50
R20
R19
R17
R18
C30
C36
C35
C34
C33
C31
C29
C32
VDD_IN
VSS_IN
SIG_IN
SIG_OUT
OUT


TITLE: LVDS TO NIM - PG. 1
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/07/02
PAGE: 15


TITLE: LVDS TO NIM - PG. 2
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/07/02
PAGE: 17
C87
C86
C85
C84
C82
C80
C83
C81
VREPNG
VNSPNG


TITLE: LVDS TO NIM - PG. 1
REV 1
ENGINEER: JOSEPH D WARNER
DATE: 2015/07/02
PAGE 18


TITLE
LVDS TO NIM - PG. 2
REV 1
ENGINEER
JOSEPH D WARNER
DATE:
2015/07/02
PAGE:
19
VSEP
VNSEP
C68
C70
C72
C73
C74
C75
C71
C69


TITLE: NI 9403 INTERFACE
REV 1
DATE: 2015/07/08
ENGINEER: JOSEPH D WARNER
PAGE: 20